

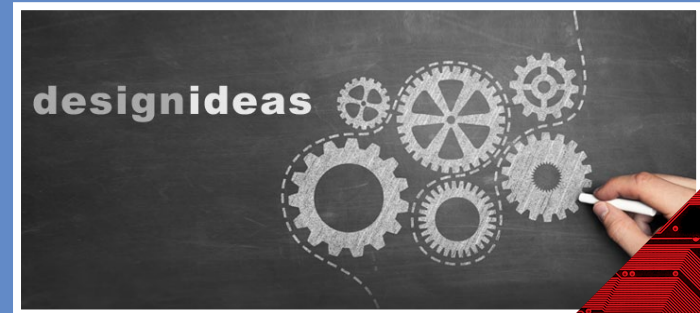
EDN

europa

DECEMBER 2015

www.edn-europe.com

Quiet power on the PCB

A close-up photograph of a copper wire coil on a printed circuit board (PCB). The wires are tightly packed and curved, creating a series of parallel ridges. The background is a blurred grey surface, likely part of the PCB or a component.

DIGIKEY.COM/EUROPE

IMMEDIATE SHIPMENT FROM THE WORLD'S LARGEST SELECTION OF ELECTRONIC COMPONENTS™



**FREE
SHIPPING
ON ORDERS
OVER €65***



**OPEN
ACCOUNTS
AVAILABLE
FOR QUALIFYING
CUSTOMERS**



**LOCAL
SALES &
TECHNICAL
SUPPORT**

1,100,000+ PRODUCTS IN STOCK | 650+ INDUSTRY-LEADING SUPPLIERS | 3.9 MILLION PARTS ONLINE

*A shipping charge of €18.00 (£12.00) will be billed on all orders of less than €65.00 (£50.00). All orders are shipped via UPS for delivery within 1-3 days (dependent on final destination). No handling fees. All prices are in euro and British pound sterling. If excessive weight or unique circumstances require deviation from this charge, customers will be contacted prior to shipping order. Digi-Key is an authorized distributor for all supplier partners. New product added daily. © 2015 Digi-Key Electronics, 701 Brooks Ave. South, Thief River Falls, MN 56701, USA

**FEATURING:
THE NEWEST PRODUCTS
AND TECHNOLOGY**



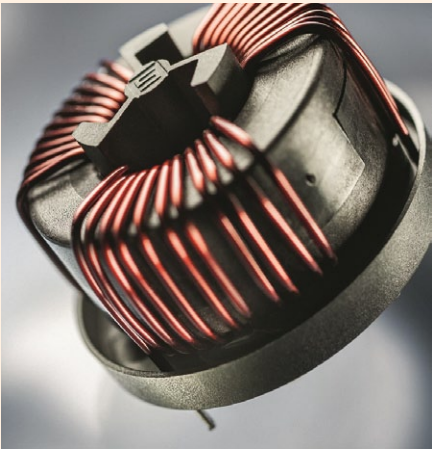
**FIND CONTACT AND ORDERING
INFORMATION FOR YOUR REGION AT
DIGIKEY.COM/EUROPE**



COVER

Suppressing noise with high currents on PCB

Aside from its visual interest, this component is a contribution from Schurter to the perennial problem of finding suitable inductors that can be PCB-mounted when the PCB is carrying the high



values of switched currents that today's power designs require. These are high-current, PCB-mounted common mode chokes for 1- and 3-phase applications

with rated currents from 10 to 50A. With open design, the chokes are light weight and compact, and suppress EMI noise from power circuits; the makers note that in smaller form factors, thermal problems and high currents can arise on the PCB. It also becomes increasingly challenging to meet EMC requirements with a filter package due to the resulting space constraints; a filter on PCB with discrete components is a good solution. Capacitors and a common mode choke, with asymmetrical effective inductance, are very effective to dampen EMI noise, and these will operate on designs handling up to 50A. More details [here](#).

FEATUREARTICLES

- 16 ARM64 vs ARM32 -- What's different for Linux programmers**
by Isa Smith, Undo Software
- 19 Push the UVM start button then hit the accelerator, Part 2**
by Doug Amos, FPGA Consultant
- 23 Understanding how a new FPGA architecture delivers throughput performance improvements**
by Mike Hutton, Altera
- 26 Taking TransferJet beyond the consumer**
by Armin Derpmanns, Toshiba and Craig Rackstraw, Icoteq
- 29 Energy is everywhere – and now it can be harvested easily**
by Franck Perronnet, Analog Devices
- 31 Don't get caught out by changing energy efficiency regulations**
by Jeff Schnabel, CUI

ONLINE THIS MONTH

Designing-in single-chip control of brushless DC motors (White paper)

A whitepaper from Micronas that discusses the advantages of using BLDC motor technology and electronics, replacing brush-type DC motor solutions 1:1 by a BLDC motor system.

EDN's columns

- 4 EDN.comment**
Exabytes need Gigawatts
- 6 Pulse**
Low-level security IP for SoCs; Smallest Raspberry Pi ever, for embedded designs; “Smarteverything”, Arduino-format development board for IoT; Imagination adds an IoT kit around MIPS-based board; MCUs mix 8051 core and accurate analogue; GPU computing promoted; Quantum computing research reported
- 21 Analog Tips**
Low-power ambient light sensing LED driver, with hibernate mode
by Chau Tran, Analog Devices
- 27 Embedded Systems**
Using Micro Python for real-time software development
by Jacob Beningo
- 45 Brian's Brain**
Anticipating CES 2016: Wearable device display trends
by Brian Dipert
- 40 Product Roundup**
BLDC motor control MCU with pre-driver; 5W transmitter IC for wireless power; RF switch presents constant impedance; 1MB flash on low-power PICs; Code analysis with functional code IDE, for ARM; Paper-thin 5 mF capacitor; Class-H audio amp; 24-bit signal chain for industrial
- 33 Design Ideas**
- 34 Software PLL syncs to line using moving-average filter**
- 37 Isolated USB-to-UART converter builds in 20 minutes for \$20**

EXABYTES NEED GIGAWATTS

One of the attention-grabbing headlines in November was “Internet to run out of power by 2020, says analyst”. This story is by my colleague Peter Clarke, and it appears in the following pages of this edition. The analysis lies within a textbook on trends in nanoelectronics, that Peter reviews ([here](#)).

The essence of the argument is contained in the table below, which is reproduced from the same book. An associated chart shows the trend in mobile internet traffic in exabytes per month and is a classic “up and to the right” shape; as with any chart, figures for future years are extrapolated but there seems little reason to doubt that the reality will be some measure of massive growth. The table shows “expected internet performance and its demand for electrical power.”

| Year | 2010 | 2015 | 2020 |
|----------------------------------|--------------|------------|-------------|
| Mobile traffic (TB/s) | 0.11 | 1.5 | 13.2 |
| Server performance (rel.) | 1 | 20 | 200 |
| Energy eff. (rel.) | 1 | 7 | 25 |
| El. power (GW) | 40 | 120 | 240 |
| PC's power (GW) | 30 | 30 | 30 |
| Mobile devices (GW) | 0.4 | 28 | 56 |
| Infrastructure (GW) | 10 | 50 | 200 |
| Total Operative El. (GW) | 80.4 | 228 | 526 |
| Embodied El. power (GW) | 80 | 228 | 526 |
| Total El. power (GW) | 160.4 | 456 | 1052 |
| Global El. power (GW) generation | 2300 | 2800 | 3300 |

This crystallises much of what we already knew, but may not have – on our own behalf – brought together as a coherent collection of thoughts. Anecdotally, even if we are not involved in designing them or any related equipment, we know that server farm capability, and power density in the racks, has been growing continuously; we have heard the tales of locating such installations close to major rivers, or beyond the Arctic Circle, to reduce the costs of dumping the heat to ambient; and of placing them adjacent to major coal fields, to cut the cost of energy transmission to the facility. (Yes; for all its technology pretensions, the internet is essentially a coal-powered phenomenon.) And we know that all of those femtosecond light pulses on ocean-spanning fibres need driving by something.

But we are getting better, are we not, in the power-efficiency of our nanometre-scale circuitry? We are; but as the reviewed book points out, not fast enough. The most superficial look at the figures in the table shows that the trends are divergent. Recall, too, that as process geometries have shrunk (for CMOS), until we reached the 10-20 nm regime each step brought gains in both density and power efficiency. In subsequent steps the density gains are there but the power gains may not be.

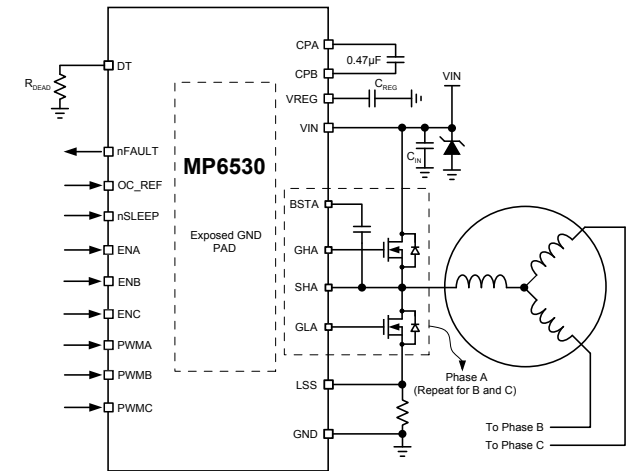
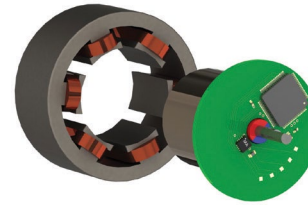
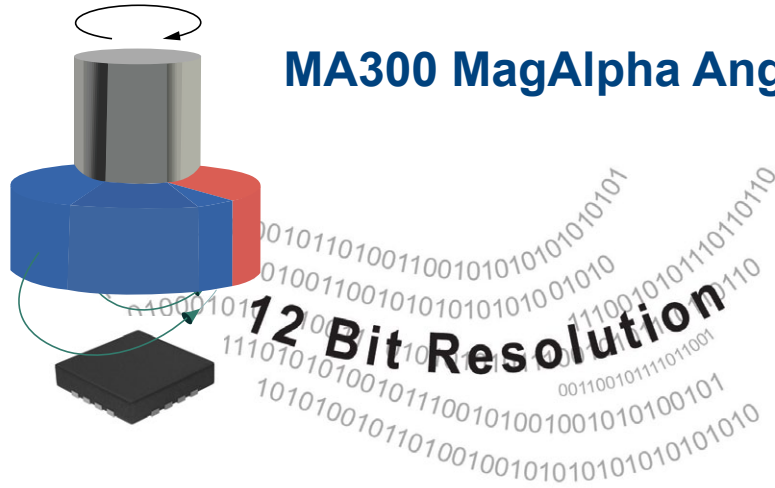
This is manifest when you have to design the regulator to feed (many) tens of Amps at sub-1V levels to a hungry multicore processor; it requires a shift of perspective to recall that someone ultimately has to pay the electricity bill for those Watt-hours, and also must try to ensure security of supply for the power.

The book – which is, as reviewer Peter Clarke observes, mainly concerned with possible technology options to resolve this conundrum – speculates that if the problem is allowed to develop, it will appear in the form of localised outages (analogous to those on a power grid) around places or events of very high usage. In fact, as far as the effect on the individual user is concerned, this is already common experience; which of us has not failed to get a phone connection (never mind a broadband stream) at a major exhibition, conference or sporting event? Power-limited rather than bandwidth-limited will be rather different phenomenon, however.

The original concept of the internet was explicitly designed to be robust in the face of degradation and impairments: if we were in a position to be objective about it, it would be interesting to see if that still remains true when [almost] unlimited numbers of video streams and social media chats push the infrastructure's power stations into brown-out.

New Angles Drive the Future

MA300 MagAlpha Angle Sensor



MP6500 Brushless Motor Driver

MagAlpha MA300 Features

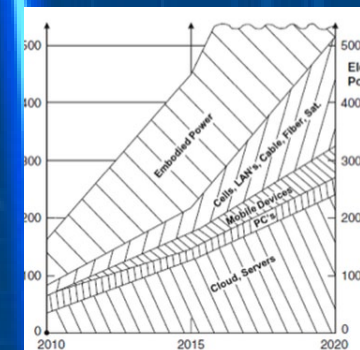
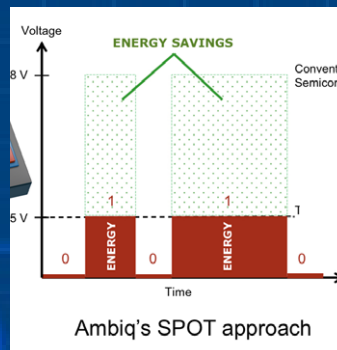
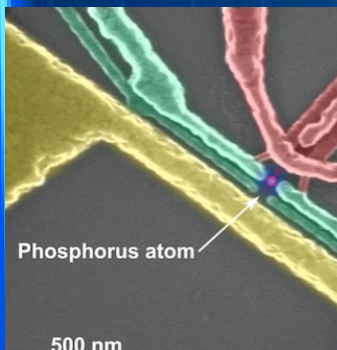
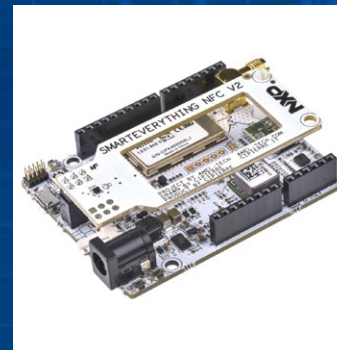
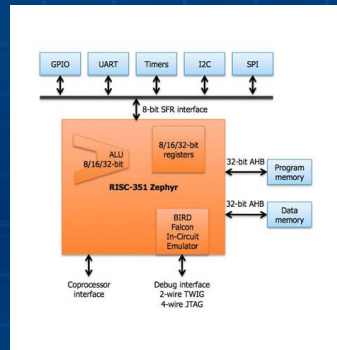
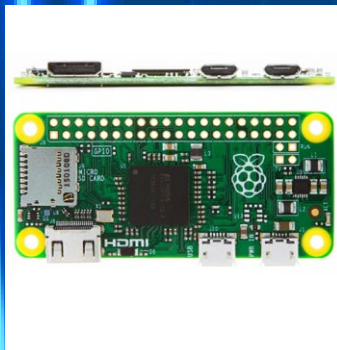
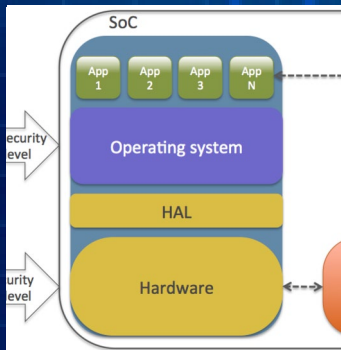
- UVW Signals for Block Commutation
- 12-Bit Resolution Absolute Angle Encoder
- 500kHz Refresh Rate
- Ultra-Low Latency: 3µs
- Serial Interface for Data Readout and Settings
- 10-Bit Incremental Output (A, B, Z)
- Built-In Linearization for Side-Shaft Mounting
- 7.5mA Supply Current

MP6530 Features

- Wide 5V to 60V Input Voltage Range
- Bootstrap Gate Driver with Trickle-Charge Circuit Supports 100% Duty Cycle Operation
- Low-Power Sleep Mode for Battery-Powered Applications
- Programmable Over-Current Protection of External MOSFETs
- Adjustable Dead-Time Control to Prevent Shoot-Through
- Thermal Shutdown and UVLO Protection
- Fault Indication Output
- Thermally Enhanced Surface-Mount Package



pulse



Internet will run out of power by 2020 warns analyst

by Peter Clarke

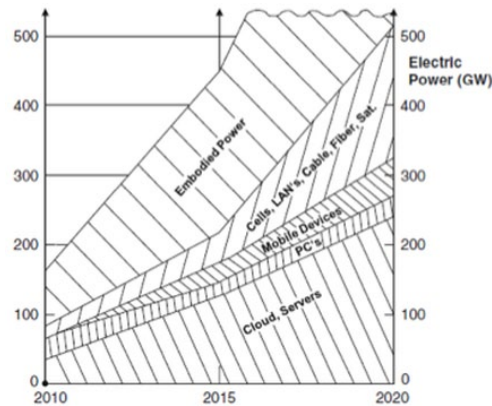
A report, "CHIPS 2020 Vol 2: New Vistas in Nanoelectronics" looks at the state-of-the-art in nanoelectronics but its most significant finding is at the global scale; that unless changes are made, the proliferation of nanoelectronics is set to produce blackout failures of the Internet by 2020 due to a lack of electrical power.

In short, the global population's eagerness to get itself and everything it owns online is leading to a data explosion that is consuming 40% more power every year and the Internet's power demand could soon rival the world's available power resources.

This is leading to fears of major Internet blackouts by as soon as 2020. Such blackouts would likely be manifested around global events such as natural or man-made catastrophes or worldwide sports coverage, says the research book's editor Bernd Hoefflinger.

Two strategies that could delay or avoid the collapse of the Internet are mentioned in the book. One is to introduce charges or taxes levied on excessive use of the Internet to curtail use of what will effectively become a limited resource. The second is to effect a series of 10x order of magnitude changes in the way in which nanoelectronics is designed, manufactured and used.

These nanoelectronic changes



Mobile Internet demand for electrical power. Source: CHIPS 2020 Vol. 2

mainly focus on digital logic and neural network architectures optimised for power consumption. Mobile Internet data doubles every 18 months, rather like a non-benign version of Moore's Law, and video data already represents 70% of Internet traffic, according to Hoefflinger, so addressing video data is a priority.

While some discussion has taken place elsewhere of a coming intelligence singularity – the point at which machines achieve an intel-

ligence superior to that of human beings – Hoefflinger has pointed out the nearer and potentially more serious energy-resource singularity.

To avoid the blackout of the Internet by 2020 and enable sustained growth of nanoelectronics beyond 2030, the world needs to embrace many radical changes, some of which are discussed in the



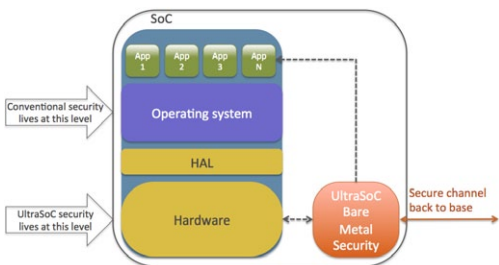
“Bare Metal Security” adds hardware system tripwire to SoCs

UltraSoC, which until now has focussed on advanced debug for systems-on-chip, has exploited the characteristics of its technology to enable a security feature that will operate at hardware level, detect any abnormalities in SoC operation – either internal failure or hacking – and alert supervisory systems.

UltraSoC's core technology is IP (intellectual property); designers of

complex, multi-core SoCs can add silicon embedded instrumentation to their designs so that when the system is being verified and debugged, any anomalous behaviour can be trapped, tracked, analysed and documented.

CEO Rupert Baines describes how, for a typical overhead (in terms of silicon area/gatecount) of 1 – 2%, the company's IP can add a “virtual, native-speed logic



analysers” - and oscilloscope functions – that can expose the root causes of system failures and performance shortfalls, when a complex chip is in bring-up and debug. The company provides

tools that monitor, for example the traffic on inter-block buses, and allow the user to define the parameters of what is expected, and what is 'normal' = and to flag any excursion of the system outside those parameters. The technology finds, in particular, inter-block and hardware/software interaction issues that are beyond the reach of the tool sets associated with any specific core.

Now, UltraSoC is extending that capability to make an in-service definition of what constitutes normal or legal behaviour. If the system departs from that, or operates outside the “box” so-defined, an alert can be generated that can (for example) set the system into a safe mode, or shutdown, or whatever the designer requires. The

event that trips the monitor could be internal (a crash, or failure of either hardware or software: or an intrusion, such as hacking). UltraSoC's IP is operating at hardware level, and can spot either case equally well; Baines says, “Never say 'never': but it would be very, very hard to hack.” He sees the

offering as of great interest to anyone building a safety-critical system, for example ECUs for automotive uses, “It is not a replacement for existing security features, but is complementary.”



TAKE A LOAD OFF
WITH CORE INDEPENDENT PERIPHERALS



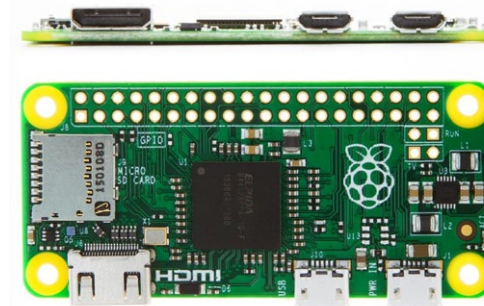
Raspberry Pi's Pi Zero board is smallest to date, for embedding

Distributor element14 adds to the Raspberry Pi product range with the smallest form factor Raspberry Pi on the market, the Raspberry Pi Zero. This board is the smallest form factor Raspberry Pi at 65 mm long by 30 mm wide and 5 mm deep.

To save space and reduce cost on the new Raspberry Pi Zero there is one Micro USB data port and a Mini HDMI port which supports full HD 1080P output. The 40pin GPIO contains the same pin out as the Raspberry Pi 2 but is unpopulated providing the flexibility to use only the connections the solution

requires. The Raspberry Pi Zero uses the single-core BCM2835 processor, which can now be over-clocked to 1 GHz, and the board has 512 MB of onboard RAM with a MicroSD port for storage.

It is expected that this model will



appeal to hobbyists and makers as well as industrial engineers looking to create solutions where size and low power consumption is at a premium such as robots, drones for capturing video, or to connect to add-ons for motor control. element14 has two Rasp-

berry Pi Zero packages available, both include a mini HDMI to HDMI adapter and Micro USB 'On the Go' adapter, and the second includes the NOOBS MicroSD card.



are saved either by using retention registers for the most fundamental ones, or by copying state to/from memory when going to or leaving retention mode for large ones such as the register file. This advanced state retention mode enables division of the power consumption by 1,000 compared to classic power modes where all core and peripheral clocks are gated (stop mode). As the impact on the embedded

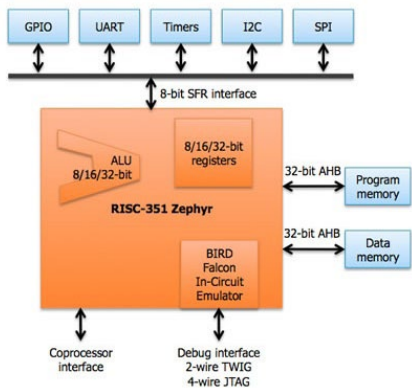
software remains a crucial concern for most users, even though the use of the advanced state of retention is a simple software increment with respect to standard retention, a library of dedicated functions is provided with Zephyr-RR in order to make the use of low-power modes straightforward.



IP builds ultra-low power 32-bit MCU with advanced power modes

Dolphin Integration (Grenoble, France) addresses demands for long battery-life in the growing market of IoT devices; energy saving becomes a paramount concern, specifically the reduction of static power consumption when

devices spend up to 99.9% of the time in an inactive mode. The RISC-351 Zephyr-RR is an energy efficient 32-bit microcontroller core that enables achieving ultra-low power consumption by combining low-power techniques with energy saving modes, suiting it for battery-operated applications which spend most of their operating time waiting for a wake-up event. In order to provide greater flexibility in power management than traditional 32-bit competitors, the RISC-351 Zephyr-RR introduces an advanced state "Retention mode" where essential registers



SmartEverything, Arduino-format dev. board for IoT, in distribution

The IoT development board from Arrow Electronics offers a wide range of sensors and communication interfaces including access to the wide-range SIGFOX communications network. Distributor RS Components has the Arduino-form-factor IoT system-on-module that comes with a range of factory-bundled I/O ports and sensors and with a highly energy-efficient wireless connectivity technology. Key elements of the SmartEvery-

thing system board are the Atmel D21 ultra-low-power MCU, based on the 32-bit ARM Cortex-M0+ processor, and a SIGFOX communications module for IoT connectivity. The SIGFOX standard is energy efficient and wide-transmission-range technology that uses UNB (Ultra Narrow Band) based radio technology and offers low data-transfer speeds of 10 to 1000 bits per second. However, very importantly, it is highly energy efficient and typically consumes



only 50 μ W compared to 5 mW for cellular communication for example, meaning significantly enhanced battery life for mobile or portable IoT devices. The SIGFOX connectivity is powered by the Telit LE51-868S high-performance module that is a certified SIGFOX gateway and covers the 863-870 MHz unlicensed ISM band. It is preloaded with the SIGFOX network protocol stack and the Telit proprietary Star Network protocol. In addition, the

Telit cloud management software enables easy connection up to the cloud.

The SmartEverything board also includes an Atmel Crypto Authentication chipset; an 868 MHz antenna; a GPS module with embedded antenna for localisation applications, which supports the GPS, QZSS, and GLONASS standards, as well as being Galileo ready; a proximity and ambient-light sensor; a capacitive digital sensor for humidity and temperature measurement; a nine-axis 3D accelerometer, 3D gyroscope and 3D magnetometer combination sensor; a MEMS-based pressure sensor; an NTAG I²C NFC (Near Field Communication) module; and a Bluetooth Low Energy (BLE) transceiver module.



8-bit, 8051-based MCUs come with high-accuracy analogue peripherals

Silicon Labs' EFM8LB1 "Laser Bee" microcontroller family offers speed, accuracy, cost-saving

integration and small footprint for optical modules – the company presents the devices as having

the highest analogue performance and peripheral integration in the 8-bit market.

They combine a high-speed ADC, multiple DACs, a highly accurate temperature sensor, two comparators and a 72 MHz 8051 core



with up to 64 kB of flash. They are packaged in 3 x 3 mm QFN, for space-constrained, performance-intensive applications such as optical modules, test and measurement instrumentation, industrial control equipment and smart sensors.

The on-chip 14-bit, 900 ksample/sec ADC includes an input sequencer and direct memory access (DMA) controller, enabling raw data collection without MCU intervention. This capability frees the MCU for other tasks, providing an increase in overall system per-

formance while enabling the MCU to enter a low-power mode for energy-saving benefits. The MCU's 72 MHz pipelined 8051-based 8-bit core can execute more than 70% of instructions in 1 to 2 clock cycles, satisfying the processing needs of high-speed optical modules and other computationally intensive applications.

EFM8LB1 MCUs integrate four configurable logic units (CLUs), enabling designers to implement combinational logic and/or synchronisers without using external components. Claimed as the smallest CLU implementation, the logic units support a variety of digital functions such as replacing system glue logic, generating special waveforms or synchronising system event triggers. Each CLU is completely programmable, to interface Laser Bee MCUs with other chips in the system. By reducing the component count and PCB space required to support glue logic, the logic units ultimately minimise BOM cost and time to market.

Many precision analogue applications include sensors or other

components that require temperature compensation. For example, laser drivers and other components in optical modules are sensitive to temperature variations. Laser Bee MCUs have a built-in,

factory-calibrated $\pm 3^{\circ}\text{C}$ accuracy temperature sensor, enabling very accurate temperature measurement without any user calibration.



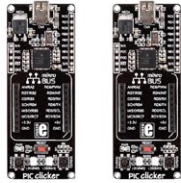
MIPS-based complete development kit for 'ground-up' IoT projects

Imagination Technologies has a development kit that has been designed from the outset for IoT applications. Creator Ci40 includes all the optimised hardware and open source software required for next-generation connected projects. It is a modular system that is easy to assemble and – Imagination asserts – even

easier to code. Developers can use it to prototype the hardware needed for an IoT application in five steps that the company has documented in a video: <https://youtu.be/8DpZlxtOIJQ> The kit comes in a single box with everything needed to build the next wireless IoT application including:



Creator Ci40 development board



6LoWPAN Clicker expansion boards



Click sensor boards

- A high-performance, low-power microcomputer acting as an IoT hub and featuring a MIPS-based chip optimised for IoT applications; the microcomputer can run a number of Linux-based operating system, including

OpenWrt, Debian as well as Brillo from Google

- Two battery-powered 6LoWPAN Clicker expansion boards with a mikroBUS (MikroElektronika) socket for adding sensors
- Three Click companion boards – a temperature sensor, a motion sensor and a relay switch (with



hundreds more available from MikroElektronika)

- FlowCloud: a complete cloud platform for connecting devices to the internet, enabling easy product registration and updates as well as access to partner-enabled services

AMD initiative to encourage spread of GPU computing

AMD has launched its 'Boltzmann Initiative', that aims to 'dramatically' reduce barriers to GPU computing, using its own AMD FirePro Graphics as a vehicle; new tools promise compute power of 28 Teraflops, for under 1 kW energy, by next year (2016). Building on its strategic investments in heterogeneous system architecture (HSA), AMD's announcement is of a suite of tools designed to ease development of high-performance, energy efficient heterogeneous computing systems. The "Boltzmann

Initiative" exploits HSA's ability to harness both central processing units (CPU) and AMD FirePro graphics processing units (GPU) for maximum compute efficiency through software. The first results of the initiative were featured at the SC15 event (Supercomputing 2015) and include the Heterogeneous Compute Compiler (HCC); a headless Linux driver and HSA runtime infrastructure for cluster-class, High Performance Computing (HPC); and the Heterogeneous-compute Interface for Portability (HIP) tool for porting CUDA-based applications to a

common C++ programming model. The tools are designed to drive application performance across markets ranging from machine learning to molecular dynamics, and from oil and gas to visual effects and computer-generated imaging.

The promise of combining multi-core, serial processing CPUs with parallel-processing GPUs to maximise compute efficiency is already being seen in the industry, as driven by the Heterogeneous Systems Architecture (HSA) Foundation that counts AMD as a founding member. One of the goals for HSA is easing the development of parallel applications through use

of higher level languages. The new AMD "Boltzmann Initiative" suite includes an HCC compiler for C++ development, greatly expanding the field of programmers who can make use of HSA. The HCC C++ compiler is a key tool in enabling developers to easily and efficiently apply the hardware resources in heterogeneous systems. The compiler offers more simplified development via single source execution, with both the CPU and GPU code in the same file. The compiler automates the placement code that executes on both processing elements for maximum execution efficiency.



Cadence hosts emulation on "datacentre-class" installations

Cadence says it, "ushers in [a] new era of datacenter-class emulation" with its Palladium Z1 Enterprise Emulation Platform. Claims include up to 5x greater emulation throughput, with an average 2.5x greater workload

efficiency than competitors; and scalability from IP blocks to full Systems-on-Chip with capacity of up to 9.2 billion gates. With enterprise-level reliability and scalability, the Palladium Z1 platform executes up to 2304 parallel

jobs and scales up to 9.2 billion gates, addressing the growing market requirement for emulation technology that can be efficiently utilized across global design teams to verify increasingly complex systems-on-chip (SoCs). Calling it, "a true datacentre resource enabling maximum utilisation," Cadence builds the platform on a rack-based blade architecture to provide 92% smaller footprint and 8X better gate density than the [prior] Palladium XP II platform. Palladium Z1 offers a unique virtual target relocation capability, and payload allocation into available resources at run time, avoiding re-compiles. With its massively parallel processor-based architecture, Palladium Z1 platform claims 4X better user granularity than its nearest competitor.

Features include:

- Less than one-third the power consumption per emulation cycle of the Palladium XP II platform. This is enabled by an up to 44% reduction in power density, an average of 2.5X better system utilisation and number of parallel



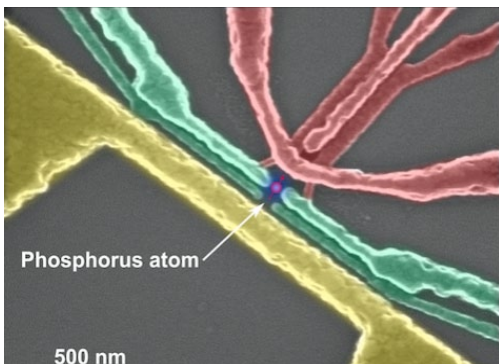
users, 5X better job queue turnaround time, up to 140 million gate per hour compile times on a single workstation, and superior debug depth and upload speeds

- Full virtualisation of the external interfaces using a unique virtual target relocation capability. This enables remote access of fully accurate real world devices as well as virtualised peripherals such as Virtual JTAG. Pre-integrated Emulation Development Kits are available for USB and PCI-Express interfaces, providing modelling accuracy, high performance and remote access. Combined with virtualisation of the databases using Virtual Verification Machine capabilities, it allows for efficient offline access of emulation runs by multiple users.



Quantum computer coding in silicon demonstrated by Australian researchers

A research team from the University of New South Wales has reported an experiment in



which manipulation of quantum entangled states – within a silicon structure fabricated by methods akin to standard nanometre-IC construction – can yield observation of all of the possible states of two quantum bits.

The engineers say they have proven – with the highest score ever obtained – that a quantum version of computer code can be written and manipulated using two quantum bits in a silicon microchip. The advance, “removes lingering doubts that such opera-


tions can be made reliably enough to allow powerful quantum computers to become a reality.”

The result, obtained by a team at UNSW, appears in the international journal, *Nature Nanotechnology*. (The complete article is [here](#); and the team's background document can be found [here](#).)

The quantum code written at UNSW is built upon quantum entanglement, which allows for seemingly counter-intuitive phenomena such as the measurement of one particle instantly affecting another – even if they are at opposite ends of the universe.

The significance of the UNSW experiment is that creating these two-particle entangled states is tantamount to writing a type of computer code that does not exist in everyday computers. It therefore demonstrates the ability to write a purely quantum version of computer code, using two quantum bits in a silicon microchip – a key plank in the quest for super-

powerful quantum computers of the future.

Complete article, here 

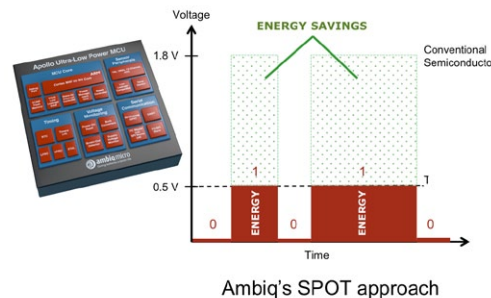
Sub-threshold logic MCU maker claims low-power benchmark lead

Ambiq Micro's ultra-low power MCU has achieved a score, on EEMBC's ULPBench, of 377, more than twice the previous

in its claim to have, “made history as a microcontroller that consumes less than half the energy of any other.”

The benchmark, created to assist embedded designers in selecting the lowest power MCU, standardises a typical low power design workload and measures the actual energy required to complete that workload. This approach normalises the many different behaviours of MCU operation such as active current, sleep current, wake-up time, core efficiency, and cache efficiency. It then synthesises this data into a single value – the amount of energy required to complete their specific application.

The Apollo MCU is based on a high-performance, 32-bit ARM Cortex-M4 processor with floating point unit. It runs at up to 24 MHz



leader's submission of 185. Ambiq Micro is the company that claims to have mastered the issues around building a production microcontroller in a sub-threshold logic process where logic levels are propagated as different voltage levels, each of which is below the 'normal' logic 'on/off' switching threshold. Ambiq is now citing the [EEMBC low power benchmark](#)

and integrates ultra-low power memory, up to 512 kB Flash and 64 kB RAM. The microcontroller comes with a set of timing peripherals, I²C/SPI master and slave ports, and a UART for communicating with peripherals and

legacy devices. The microcontroller consumes 34 μ A/MHz executing instructions from Flash, and sleep-mode currents can be as low as 140 nA. A video is at; <http://youtu.be/Ju7V16Hhq8s>



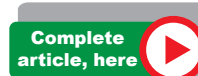
Free, unrestricted IDE for ARM links to SaaS subscription tools

Atollic says it, “unifies [the] fragmented ARM tools market with free no limitations TrueSTUDIO C/C++ IDE.” The release is a, “completely free, commercial-quality IDE without code-size or device usage limitations. This

gives the ARM development community a free-of-charge tool that everyone can standardise on.” The tool is free to download, use and share. No registration is required. Atollic asserts that there is fragmentation [in the tools area]

caused by a vast amount of similar development tools with little differentiation. They all offer basic edit/compile/debug capabilities but often suffer from poor usability experiences due to the tool being less tightly integrated than a unified professional tool chain. Others may be locked to a single chip vendor which limits the breath of target support. The lack of standardisation often leads to duplication of efforts, code portability challenges, and increased cost for middleware suppliers and development consultants. In combination with the launch of

the free TrueSTUDIO Lite, Atollic is introducing a low-cost upgrade path to TrueSTUDIO Pro, the company's flagship development tool which includes static code analysis, and advanced debugging capabilities such as event-, data- and instruction-tracing, live variable watch, crash analysis, and RTOS-aware debugging. The Pro edition also includes full technical support. Developers will now have the option to add these capabilities with a low-cost, “pay as you go” subscription option.



Mixed signal oscilloscopes claim top performance for entry-level prices

Rohde & Schwarz has introduced the entry-level R&S HMO1202 mixed signal oscilloscopes that offer a bandwidth of up to 300 MHz coupled with comprehensive math and FFT analysis functions which make the scopes suitable for professional analysis of digital signals.

Two analogue and eight digital channels, a sampling rate up to 2 Gsample/sec, a memory depth up to 2 Msample, and a true vertical sensitivity of 1 mV/div are all featured in an instrument which is priced at under €2,000. The mixed signal oscilloscopes are able to analyse serial SPI

buses on digital channels while simultaneously monitoring two analogue signals referenced to the transmitted SPI data. All that is needed is the separately available R&S HO3508 logic probe from Rohde & Schwarz, which is compatible with all HMO oscilloscopes. Rohde & Schwarz has packed numerous math functions into the oscilloscopes, from simple standard operations such as add, subtract and divide to logarithmic differentiation and integration of waveforms. A formula editor is also available for entering a variety of calculation functions, such as integrating waveforms to determine the charge on a capacitor. The built-in FFT analysis functions with 128 kpoints are equivalent to those found on larger oscilloscopes. Time domain signal,

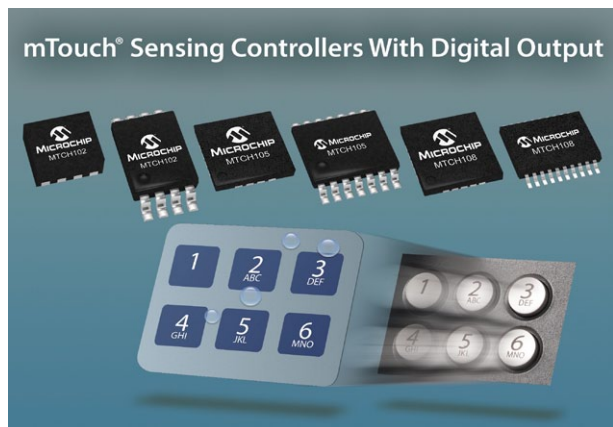
measurement window, result and analysis range are displayed in a single window, facilitating spectral measurements. FFT analysis can even be performed on recorded signals, making it possible to analyse segments of interest by varying the window width. The instrument is available in three different models, the HMO1212 with a bandwidth of 100 MHz, the HMO1222 with a bandwidth of 200 MHz and the HMO1232 with a bandwidth of 300 MHz. Upgrade vouchers offered by Rohde & Schwarz allow users to upgrade the instruments even long after the purchase date. A voucher is used to obtain a license key to extend the bandwidth of the HMO1202 from 100 MHz to 200 MHz or to 300 MHz.



Replace mechanical buttons with capacitive touch

Applicable to cost-sensitive, low-power applications, Microchip Technology's mTouch

controllers enable embedded developers to integrate proximity and touch-sensing technology without



writing any software; multi-stage noise filtering algorithms support gloved operation. Microchip has added to its MTCH10x mTouch sensing portfolio with the turnkey MTCH102-5-8 capacitive touch controllers. In a hardware-only configuration, these 2, 5 and 8-channel controllers replace mechanical buttons with a simple digital output, to add proximity and touch detection to any application that is constrained by size, power or cost. To achieve high reliability and more sensitive touch performance, including opera-

tion through a glove, the controllers come with advanced multi-stage noise filtering algorithms. The controllers support a range of touch-sensor shapes and sizes, with automatic compensation for environmental conditions, and provide reliable operation in the presence of water. Active guarding increases proximity-sensing sensitivity and makes the electronic design robust, even with long board traces to the touch sensors.



LEDLighting

ARM64 VS ARM32 -- WHAT'S DIFFERENT FOR LINUX PROGRAMMERS

By Isa Smith, Undo Software

When ARM introduced 64-bit support to its architecture, it aimed for compatibility with prior 32-bit software. But for Linux programmers, there remain some significant differences that can affect code behaviour. Here are some we found and the workarounds we developed for them.

I had originally planned to call this article “What’s NEW in ARMv8 for Linux Programmers?” However, I think “what’s different” is much more apt. And, just for the record, by “ARMv8-A” I mean AArch64, with the A64 instruction set, also known as arm64 or ARM64. I’ve used AArch64 registers in the examples, but many of the issues I’ve described also happen in the ARMv8-A 32-bit execution state.

To help frame the problems discussed here, let me start by giving a little background on the sort of codebase we have here at [Undo](#). Our core technology is a record and replay engine, which works by recording all non-deterministic input to a program and uses just-in-time compilation (JIT) to keep track of the program state. Our technology started on x86 (32 and 64-bit) and had progressed to have fairly complete, maturing support on ARM 32-bit when we

began adapting it to work on AArch64. I joined the company after almost all of the low hanging fruit had been grabbed (as well as many rather higher up the tree, to be fair) leaving us with some tricky problems to tackle when it came to moving to ARMv8.

This leads me to my first simple, but possibly helpful, observation: ARM64 is much more similar to ARM 32-bit (a.k.a. AArch32) than it is to x86. ARM64 is still quite RISC (though the cryptographic acceleration instructions do lead to raised eyebrows in a RISC architecture). So I don’t intend to try to cover the many differences between x86 and either ARM version. Nor do I want to rehash the differences between AArch32 and AArch64 -- there are already [good resources](#) to explore those differences.

Also, a lot of ARM versus ARM64 resources focus on the instruction set and architectural differences. These differences are not really relevant to most Linux user space application developers, beyond the very obvious, such as “your pointers are bigger.” But, as we discovered, there are differences important to Linux user space developers, four of which I’ll discuss here. These differences fall into several

categories, some falling into more than one category. The categories are:

- Differences due to migrating to use a fairly new kernel version.
- Differences due to the architecture and instruction set (where this is relevant to user space programmers).
- *ptrace* differences. We use *ptrace* a lot, so this was very important to us.

I will try to use the following format in the next sections:

- A brief explanation of the area.
- What is the difference? Why is this different? (Sometimes it is easier to understand a change in behaviour by looking at a few assembly instructions than it is from a wordy description, so I’ll provide that code.)
- How did we encounter it?
- How did we overcome it?
- Where to find out more information.

1. Changes to *ptrace*

ptrace provides process tracing capabilities to user space programs.

There have been a number of changes to the requests accepted by *ptrace()*. These changes produce the most pleasant of all incompatibilities to analyse: compilation errors. Our

error reports were for undefined symbols `PTRACE_GETREGS` (for general registers), `PTRACE_GETFPREGS` (for floating point and SIMD registers), and `PTRACE_GETHBPREGS` (for hardware breakpoint registers), as well as the SET versions of these requests.

The [man](#) page for `ptrace` was no help at all in resolving these errors, so we dug deeper. We had a look at the kernel source, and it turns out that usually there is an architecture-independent `ptrace` code path (`ptrace_request()` in `kernel/ptrace.c`), and separate architecture-dependent paths (e.g. `arch_ptrace()` in `arch/arm/kernel/ptrace.c`). Although the arm64 version has a `compat_arch_ptrace` for AArch32 applications, the arm64 `arch_ptrace()` directly calls `ptrace_request()` and does not add any additional `ptrace` request types.

The solution is to use `PTRACE_GETREGSET` and `PTRACE_SETREGSET` with various different arguments to read these registers.

Here is a table of the GETREGS-style request and the closest equivalent GETREGSET request. Different REGSETs are acquired through different arguments to `addr_ptrace()` argument.

Note that `NT_ARM_HW_BREAK` and `NT_ARM_HW_WATCH` behave identically in a GETREGSET request.

| ARM 32-bit | AArch64 |
|------------|-----------------|
| GETREGS | NT_PRSTATUS |
| GETFPREGS | NT_PRFPREG |
| GETHPBREGS | NT_ARM_HW_BREAK |
| | NT_ARM_HW_WATCH |

Table 1. ARM 32-bit and closest equivalent AArch64 ptrace requests.

Using GETREGSET is not as simple as using GETREGS, though. For a GETREGS request like this:

```
ptrace(PTRACE_GETREGS, 0, 0, regs);
```

GETREGSET would look like this:

```
struct
{
    void*    buf;
    size_t  len;
} my_iovec = { regs, sizeof(*regs)};

ptrace(PTRACE_GETREGSET, 0, (void*)
NT_PRSTATUS, &my_iovec);
```

Note, too, that I have said “the closest equivalent GETREGSET request.” Naturally, the

AArch64 register set is different from the ARM 32-bit one, but there are more differences between the two beyond the register set.

Figure 1 shows a diagram of the registers returned from an ARM 32-bit GETREGS and AArch64 GETREGSET instruction.

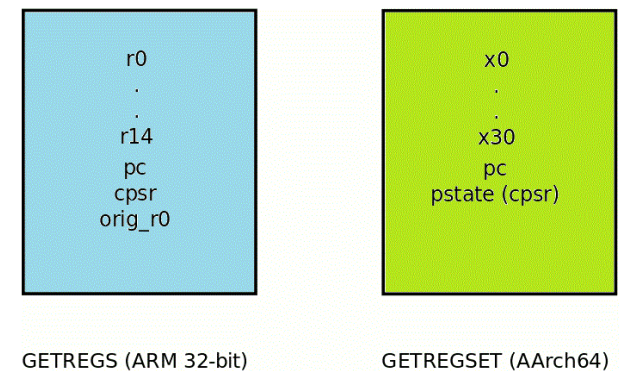


Figure 1. GETREGS and GETREGSET.

ARM64 & LINUX

Those familiar with AArch64 may notice that with GETREGSET we've been given a "cpsr" register, yet the hardware architecture does not have one. What's returned with GETREGSET has been synthesised into a cpsr-like layout from the individually accessible fields on AArch64.

A more notable difference between the two is the lack of orig_r0 (or orig_x0) for GETREGSET. This lack has to do with syscalls. On ARM 32-bit, a syscall number gets placed in r7 and the syscall arguments are placed in the argument registers r0-r3 prior to a *syscall(SVC)* instruction. The value returned from the syscall is located in r0 (as per the usual APCS, r7 in exceptional circumstances). After the kernel returns from the *syscall*, orig_r0 provides the original first argument to the *syscall* (which had been overwritten by the return value).

I actually don't know what use a "normal" application is supposed to make of this original first argument. We use it for our support of *restart_syscall*, where the return value is `ERESTART_RESTARTBLOCK`.

Unfortunately the lack of orig_x0 is a problem

for us that we have yet to resolve in all circumstances. If we have recorded the entry to the *syscall*, then we have all the information we need. However, if we have attached during a *restart_syscall*, then we do not know the original value of x0. Our only option is to allow the kernel to restart the *syscall*, but this restart is inefficient for us as we can't optimise the recording of the *syscall*.

Returning to the subject of GETREGS versus GETREGSET: `GETHBPREGS` and `NT_ARM_HW_BREAK` are also significantly different. For a `GETHBPREGS` request, you use the *addr* field in the *ptrace* call to request a particular hardware breakpoint register. `NT_ARM_HW_BREAK` returns *all* hardware breakpoint registers.

The best place to look for more information on these *ptrace* differences is to examine the AArch64 *ptrace* source file: `arch/arm64/kernel/ptrace.c`

Isa Smith continues her article with a consideration of *Increased use of locks* - [click for pdf](#)



Download PDF
of Article



Find ARM 64
on EETsearch



PUSH THE UVM START BUTTON THEN HIT THE ACCELERATOR, PART 2

By Doug Amos, FPGA Consultant

Editor's note; This commences part 2 of the article, of which part 1 appears on the EDN-Europe website, [here](#). For convenience, click the link at the bottom of page 20 to access a single pdf file of the complete article.

Faster interfaces using transactors

Taking a look at the top-level ports of a typical DUT, in many cases these will be standard peripheral or bus interfaces (such as USB, SATA, APB etc.); the behaviour of each is well understood. We can use this known behaviour to agree short cuts in the communication between simulator and hardware. For example, instead of relying on the simulator to drive every signal change for the writing of a data value over a standard port, we place some extra hardware alongside the DUT in the FPGA(s) which makes those changes for us locally. This is shown in Figure 3 as a BFM, or Bus Functional Model.

A single command or function call on the simulator side could then initiate all the necessary changes on the hardware side. The mechanism by which this all happens is called a transactor, and in Figure 3 this comprises the BFM interface on the simulator side, a transaction layer and the BFM in the FPGA hardware.

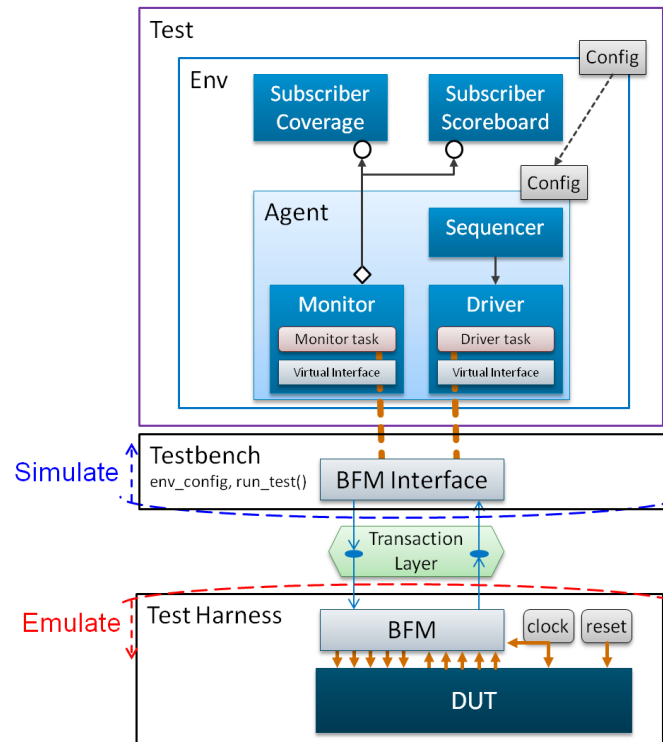


Figure 3. Partitioning using a transactor

Not only does the transactor simplify the communication, it also allows the hardware to run faster because it is not reliant on slavishly following signal-by-signal events in the simulator. If all the interfaces between the simulator

and the DUT employ the relevant transactor, then we can achieve greater acceleration overall.

UVM already employs transactional level communications, but how do we convert our simulator-only UVM test environment to use transactors and FPGA-based hardware?

Linking UVM and FPGA

Preferably, we should have written our UVM/SystemVerilog testbench in a style that allows easy inclusion of transactors. As it happens, the style recommended by Easier UVM is exactly such a style, and with a few simple substitutions, the verification team can re-compile and run the design using FPGA-based acceleration. In Aldec's case, this adaptation of the UVM is performed mostly automatically in its Design Verification Manager (DVM) tool.

At the heart of a transactor-based acceleration is the representation of interface transactions as function calls within UVM agents. The UVM agent's driver makes a single function call, resulting in – sometimes – hundreds of signal changes in the hardware, at a much higher clock rate than the simulator event rate. The same effect is happening on outputs from the DUT into the simulator via the UVM agent's monitors. It is this ratio of calls-to-signal changes that increases throughput.

VERIFICATION

We might also think of the boundary as dividing the timed and untimed domains, between events and clocks, and the clock is never used to synchronise communication across the boundary.

We see this simplified in Figure 4, which also differentiates the two domains by the languages used to describe them, i.e. a Hardware Verification Language (HVL) - in this case SystemVerilog on the one side; and the transactors written in Hardware Description Language (HDL) such as Verilog or VHDL, on the other.

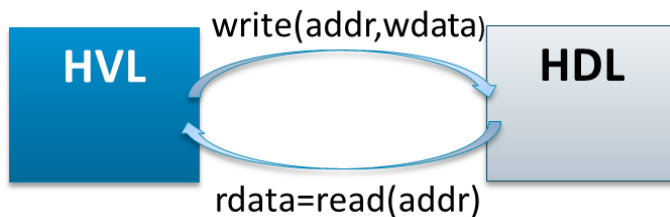


Figure 4. HVL and HDL communication via function calls

Of course, SystemVerilog can be employed as both an HDL and an HVL, but if there are any SystemVerilog items appearing on the right-hand side of Figure 4 then it must be synthesisable, or somehow interpreted as such during set-up.

We wouldn't get far without SCE-MI (and DPI-C)

The approach of HVL-HDL partitioning has been captured in Accelera's Standard Co-Emulation Modeling Interface (SCE-MI) which that body describe as "allowing a model developed for simulation to run in an emulation environment and vice versa." Aldec follows the SCE-MI standard which recommends that the cross-boundary function calls are made via SystemVerilog's Direct Programming Interface (DPI), which allows it to communicate with other programming languages. In the case of the C language, we term this DPI-C for short.

DPI-C allows us to make calls to externally defined (and imported) C functions from within a SystemVerilog testbench, and to export SystemVerilog items allowing them to be ac-

cessed from C. This is very helpful for accelerating UVM as we can use DPI-C as the wrapper between the testbench calls and the transactors which will be synthesised along with the DUT into FPGA. We can see this in Figure 5 (note the naming convention used by Aldec).

Part 2 of this article concludes [here](#); or click below for the pdf of the complete article.

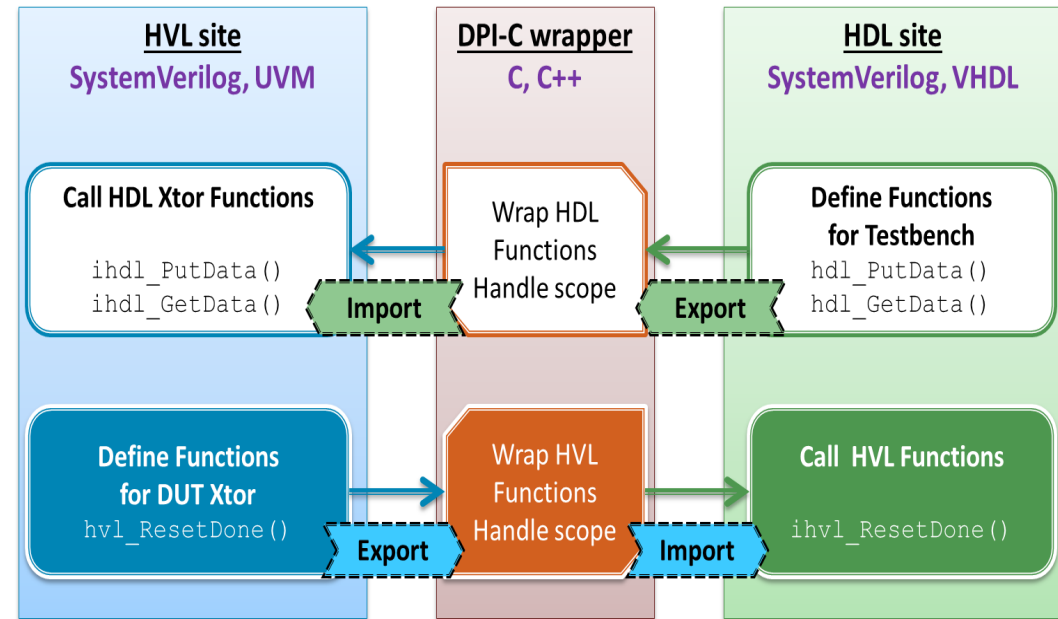


Figure 5. DPI-C acts as the boundary between simulator and hardware



Download PDF
of Article



Find UVM & FPGA
on EETsearch

LOW-POWER AMBIENT LIGHT SENSING LED DRIVER, WITH HIBERNATE MODE

BY CHAU TRAN

This circuit of only a few components is powered by two AA batteries and features a mode that extends its power savings.

Imagine a smart light switch which not only automatically turns itself on when it gets dark, but also adjusts its level of illumination to compensate for the ambient level of darkness. For example if this switch were applied to car headlights, the headlights would automatically come on at dusk,

and gradually get brighter as the car's environment gets darker. The circuit shown in Figure 1 performs this function: it automatically adjusts the LED's output light density in proportion to the ambient lighting conditions as sensed by the LDR.

The circuit employs an ADA4807, low power, low noise, rail-to-rail voltage feedback operational amplifier, an LDR, an LED, and a few passive components. The LDR, or light-dependent-resistor,

is the main sensor of the circuit while the op-amp is a square wave generator and also serves as an LED driver because it can typically source or sink a reasonable ± 40 mA linear output current. The LED, or light emitting diode, will turn on if there is more than 2V of forward bias across it. The resistance of a photo-resistor or other LDR varies with light

intensity. An LDR's resistance is several mega-Ohms in darkness, decreasing to a few hundred Ohms in bright light. This allows the circuit to distinguish between direct sunlight and total darkness and everything in between.

Generally, the amplifier is connected as an oscillator; the positive feedback loop and the negative feedback loop causes the amplifier to oscillate automatically. When the capacitor reaches each threshold, the charging source is switched from the negative power supply to the positive power supply, and vice versa.

There is an RC circuit between the inverting input and the output of the comparator. Because of this, the inverting input of the comparator asymptotically approaches the comparator output voltage with a time constant RC. This time constant RC determines the frequency of the oscillation.

$$f = 1 / (2 \cdot \ln(3) \cdot R \cdot C)$$

The duty cycle of the signal can be adjusted by changing the ratio of resistance of R1 to the resistance of the LDR. If those two resistances are equal the output is symmetrical (50% duty cycle). However, the resistance of the LDR is light sensitive; therefore, variations in ambient light will change its resistance value which directly affects the duty cycle of the oscillation. The frequency of the square wave oscillation is higher than that which human eyes can detect therefore one won't see the LED flashing on and off. One only observes the brightness of the LED as a function of ambient light density as driven by the duty cycle of the square wave oscillation.

The output of the driver swings as close as 40 mV to the +/- rail voltage with a linear output current source of 50 mA, typically.

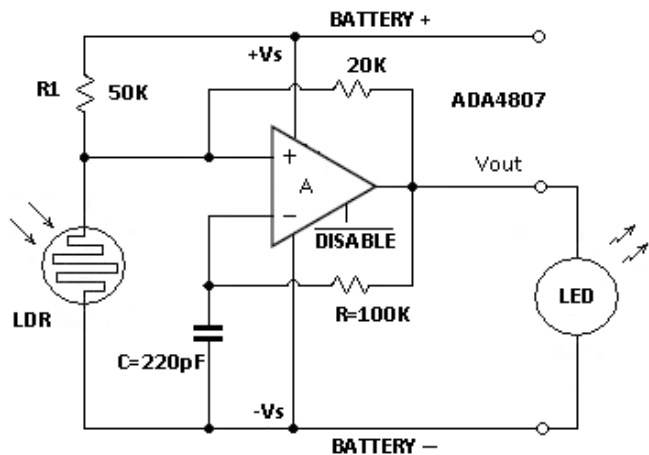


Figure 1. An automatic light sensitive circuit.



Analog Tips

For energy savings when the circuit is not in use, it can be put into “hibernation mode” by pulling the DISABLE pin low which will shut down the op-amp within a few hundred nanoseconds. Once the circuit is disabled the remaining system operating current mostly comes from the resistor divider R1 and LDR, and as such, the supply current of the op-amp is reduced from 1 mA to 2 μ A. The output enters a high impedance state but it takes less than a half micro second to enable it again.

When active, the op-amp’s power consumption is 3 mW. In hibernate mode, the typical supply current dramatically reduces to 2 μ A and the power consumption decreases to 6 μ W. This is a ratio in power savings of 500:1. The disable pins make switching between the two modes easy. With an extremely fast turn on and turn off time, there is virtually no waiting time in switching between the two operations.

Figure 3 shows three different stages of lighting conditions. When the environment is well lit, the output is low (0) as shown by the green trace, marked “Bright”, and of course, the LED is off. When the environment begins to darken as shown by the blue trace, marked “Little Dark”, the duty cycle is at about 15% and the LED’s output light is dim. When the envi-

ronmental is very dark, as shown by the red trace marked “Dark”, the output is on longer than it is off and the LED’s output is very bright.

This type of circuit can be used in many lighting applications. As it exhibits low power consumption, has a rail to rail input/output, and features a useful disable mode, this circuit can be powered by just two AA batteries for use in very power sensitive applications. For higher-power lighting applications,

one can add a power transistor for driving a heavier load consisting of an array of LEDs.

Chau Tran [chau.tran@analog.com] joined Analog Devices in 1984 and works in the Instrumentation Precision Technology (IPT) Group in Wilmington, MA. In 1990, he graduated with an MSEE degree from Tufts University. Chau holds more than 10 patents and has authored more than 20 technical articles.

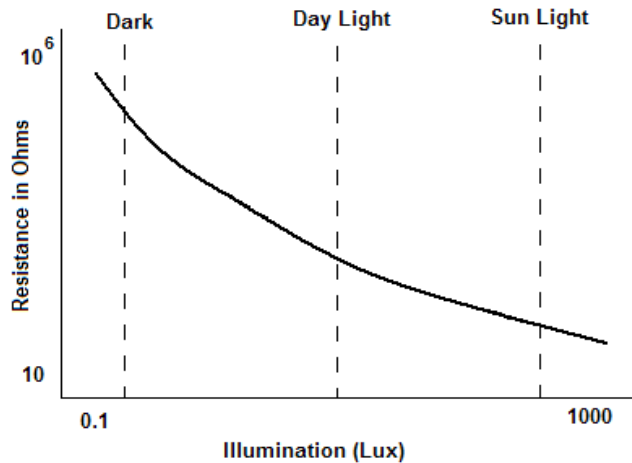


Figure 2. The characteristic of the photo-resistor.

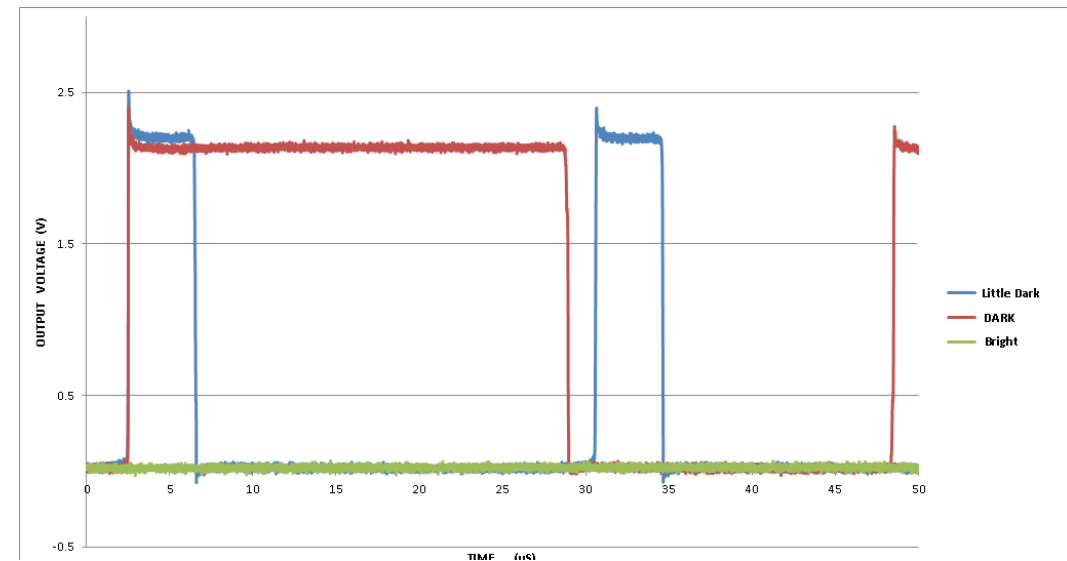


Figure 3. Waveforms at output with different light densities

UNDERSTANDING HOW A NEW FPGA ARCHITECTURE DELIVERS THROUGHPUT PERFORMANCE IMPROVEMENTS

By Mike Hutton, Altera

In order to keep pace with the increasing demand for increased device performance, IC designs have to keep several steps ahead in order to exploit market demands by matching it with product availability

Widely experienced across all sectors of semiconductor design, nowhere is the pressure as great as in the high performance computing area, where the need to deliver increased network bandwidth and throughput are growing exponentially. In this sector many designs employ FPGAs to deliver these performance expectations but even with advanced architectures, designers have had to resort to implementing their designs using extremely wide on-chip buses, often up to 2,048 bits wide.

Routing architectures can make the wires more efficient by using hierarchy and optimisation techniques. However, doubling the number of wires simply adds die area and increases power dissipation. The traditional methodology of building register-look-up table (LUT) pairs that is present in all existing FPGA core architectures means that logic is sacrificed to reach the added pipeline registers. Pipelining in conventional architectures also incurs a delay cost because a signal needs to be routed into and

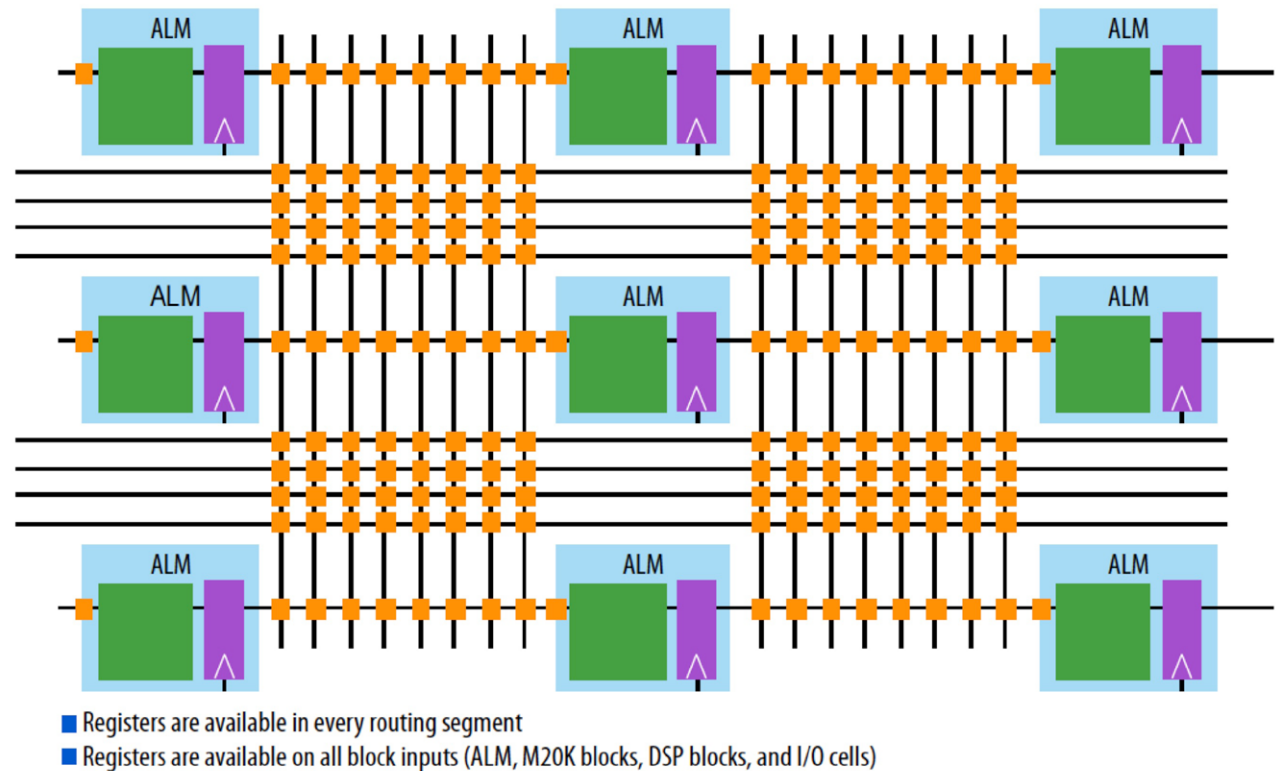


Figure 1. "Registers Everywhere" approach employed in the HyperFlex architecture

PROGRAMMABLE LOGIC

out of a logic block. The result is diminishing returns for the pipelining technique, especially when routing delays dominate the total delay.

Another challenge is that of minimising clock variation and skew since it becomes increasingly significant as speeds increase. Pushing speeds above 500 MHz, a new clocking solution is required – rather than adding more balanced clock trees.

Recently Altera launched a new architecture called HyperFlex for its FPGAs that uses a number of new features that collectively provide a doubling of core performance. To reap the performance improvement developers need to apply a number of techniques that should already be familiar to them such as register retiming, pipelining and design optimisation. The combination of these techniques together with the architectural improvements account for the performance improvements. The essential architectural change is one of adding many additional registers (Hyper-Registers) throughout every interconnect routing segment and at the inputs to every functional block. Use of these registers allows developers to re-time critical paths and use pipeline registers to remove

routing delays. And this approach of bypassable retiming and pipelining registers breaks the link between the functional registers in the adaptive logic module (ALM) and the registers used for re-timing and pipelining.

All routing segments [in devices with this architecture] have an optional Hyper-Register built into the programmable routing multiplexer that allows the routing segment to be registered or combinational. These Hyper-Registers are available everywhere throughout the core fabric, as shown in Figure 1. The Hyper-Registers are represented by the small squares at the intersection of every horizontal and vertical routing segment.

With this architecture, there is no need to use an adaptive logic module to find a pipeline register. Every horizontal and vertical interconnect line in the device contains a Hyper-Register that can be turned on or off by configuring the FPGA. Hyper-Registers are simple, one-input one-output bypassable registers without routing multiplexers on the input.

Click for the full article which goes on to give examples of how the modified architecture benefits design optimisation.



**Download PDF
of Article**



**Find FPGA Architecture
on EETsearch**

TAKING TRANSFERJET BEYOND THE CONSUMER

By Armin Derpmanns, Toshiba and Craig Rackstraw, Icoteq

Using fast, simple and secure wireless data transfer in industrial, manufacturing, commercial and other non-consumer applications

Combining the speed of UWB with the ease of NFC, TransferJet is gaining momentum as a method of quickly and easily transferring high volumes of data from one consumer device, such as a smartphone or digital camera, to another. However, the speed, security, reliability and cable-free benefits that the technology offers are attractive not only to consumers but also to a variety of industrial, medical, automotive and commercial user communities.

The drive to share files faster

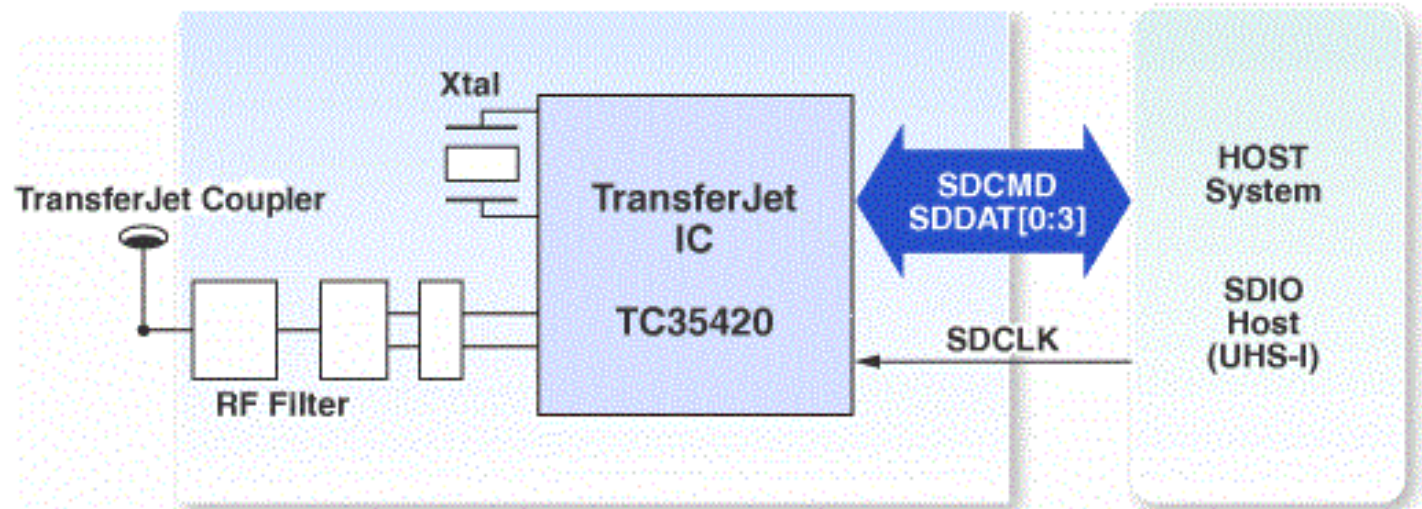
Transferring small quantities of data, such as financial transaction data, directly between devices has become much easier with the advent of technologies such as NFC. On the other hand, users looking to share large files, such as digital camera images or HD video clips, have typically had to choose from less user-friendly options: connect to a Wi-Fi network, find a USB cable, or remove the device's media card.

TransferJet allows convenient point-to-point connection for wireless exchange of large files,

eliminating any need to connect to a network, attach a cable or swap removable media. The maximum transmission rate of 560 Mbit/sec translates into an effective data throughput of 375 Mbit/sec, which is enough to transfer a 20 second HD video clip in one second. The system can adjust the transmission rate depending on the wireless environment, to ensure robust communication even when conditions are unfavourable.

Two TransferJet devices quickly establish a connection when brought together; that is, into

close proximity, or touched. The short communication range of only a few centimetres eliminates challenges such as multipath fading or shadowing, thereby saving the equalisation and signal-processing circuitry needed for longer-range solutions. Touch also allows the TransferJet protocol to assume that the user has authorised the connection, which allows the search, discovery, selection, authentication and connection procedures that are common to wireless communication protocols to be performed automatically with no need for further action. Once the connection is made, the ap-



INDUSTRIAL INTERFACES

plication can then determine the next action, such as transferring a file, querying the user, or displaying a menu.

TransferJet overview

TransferJet operates at a centre frequency of 4.48 GHz, in the same license-free frequency band as Ultra-Wideband (UWB), and occupies a bandwidth of 560 MHz. The short transmission distances of only a few centimetres permit maximum RF power of only -70 dBm/MHz, which ensures compliance with the low-power radio regulations in place throughout the Americas, Europe and the Far East.

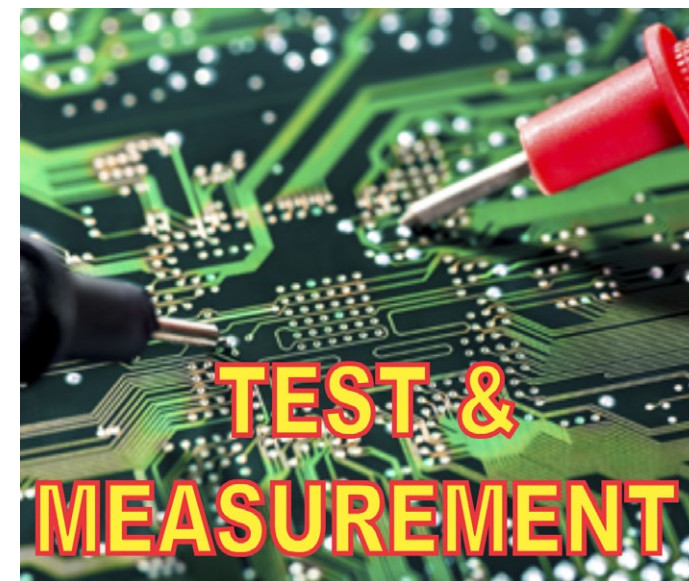
The TransferJet specifications define the physical Layer (PHY), connection layer (CNL) and protocol conversion layer (PCL) corresponding to layers 1, 2, 4 and 5 of the OSI model. Since there is no network connection, the OSI layer 3 is not required.

TransferJet supports two well defined protocols, taking advantage of the Object Exchange (Obex) Inbox Service for file exchange, and Small Computer Systems Interface (SCSI) with Obex Folder Browsing Service for file transfer.

As far as security is concerned, there is little risk of any security threat from a distant location since TransferJet communication occurs over such short distances. For this reason, TransferJet is able to operate without integrated link layer security thereby saving power, cost and complexity. Encryption can be added at the application level, in situations where the integrity of the transferred files is critical. In addition, since each device has a unique ID, any device that attempts to establish a connection can be readily identified.

To limit communication distance and ensure that signal energy drops off sharply outside the desired range, TransferJet devices utilise a coupler that behaves unlike a conventional antenna. The coupler effectively suppresses far-field components while emphasising the near field signal strength. Moreover, the coupler sets up an un-polarised longitudinal component in the near field that allows easier alignment of the two connected devices for optimum communication.

Click below for the full article PDF which expands on development tools and use cases.



**Download PDF
of Article**



**Find TransferJet
on EETsearch**

EMBEDDED SYSTEMS

USING MICRO PYTHON FOR REAL-TIME SOFTWARE DEVELOPMENT

BY JACOB BENINGO

While languages such as Ada and C++ have gained some adoption in certain circles, for the most part embedded software is still dominated by the procedural and dangerous C programming language. A few years ago, though, an interesting movement began to port Python for use on microcontrollers.

Recently, the Python 3.5 port, known as Micro Python, has been gaining popularity and adoption amongst hobbyists and professional developers alike.

The [Micro Python organisation](#) describes Micro Python as “a lean and fast implementation of the [Python 3](#) programming language that is optimised to run on a microcontroller.” Micro Python runs on the bare metal and uses a custom class known as *pyb* to access the low level peripherals of the host microcontroller. The *pyb* class provides developers with abstracted access to interrupts, timers, LEDs, ADC, PWM, I²C, SPI, and CAN to name a few peripherals.

For developers who feel these objects don't provide enough control over the microcon-

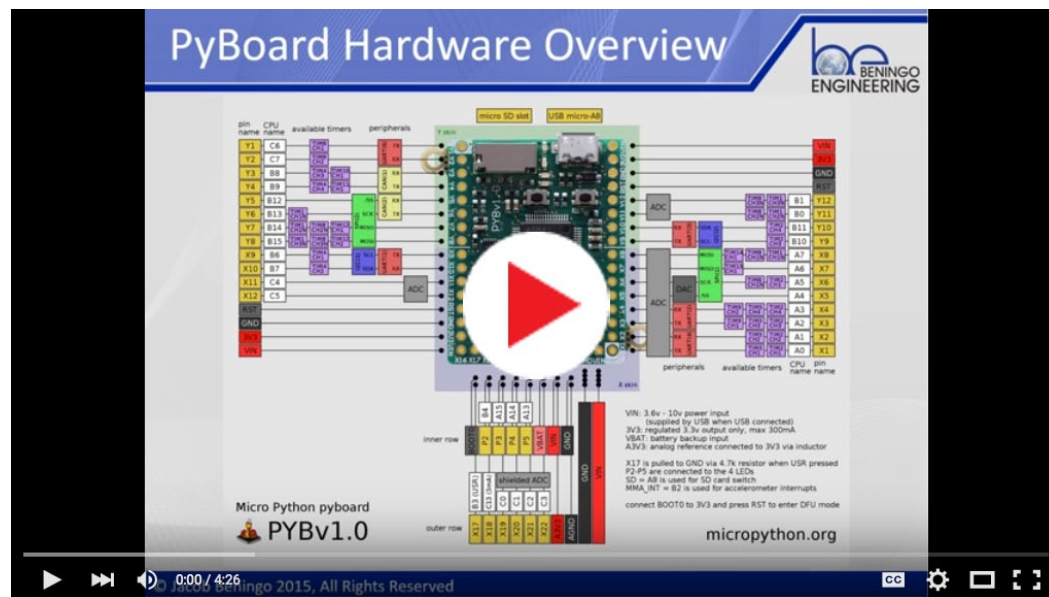
troller, there also exists a C API that can be used to wade through the abstractions and directly access the microcontroller registers.

Many different ports of Micro Python already exist but the primary flagship runs on the [PyBoard](#) development platform. The PyBoard is based on an STM32F405RG microcontroller that contains an ARM

Cortex-M4 core running at 168 MHz with a hardware floating point accelerator. The microcontroller has 1 MB of Flash and 192 kB of RAM. Where 1 MB of flash space isn't enough, developers can use an external high density micro SD card to store Python scripts.

Micro Python offers developers with an easy to use, human readable programming language that abstracts out the hardware layer and allows developers to focus on the application. Python has long been a popular and portable programming language well known for its interpretive language features and its easy learning curve. The demand for Python developers has been steadily growing and the language has found uses across many industries and technical sectors. The portability of Python itself allows algorithms to be developed and tested long before target hardware is available to test.

Developers also shouldn't forget that Python is not just a scripting language but also an object orienting programming language. Object Oriented Programming techniques can be used to create software that is portable, maintainable, modular, and extensible. Dust off those old OOP textbooks because inheritance and polymorphism are back on the table!



EMBEDDED SYSTEMS

Seasoned engineers may be hesitant to consider Micro Python as an option. After all, between garbage collection and other background tasks can Micro Python really offer real-time response? Over the past several months I've been testing and probing the real-time behaviour of Micro Python as it behaves on the PyBoard and so far it has held up really well. The hardware floating point accelerator ensures fast and accurate floating point calculations with little to no impact on real-time performance.

The use of proper design techniques through the use of interrupts and timers allow most real-time deadlines to be met with ease. I even designed a scheduler and loaded it up with tasks to read analogue sensors, drive a motor, and read SPI and I²C sensors, all while calculating a complex algorithm. Yes, I even implemented try/except/finally error handling, error and data logging while transmitting data off board via UART to perform real-time plotting! So far there hasn't been so much as a hiccup.

Another sticky point one may consider concerning Micro Python is that the PyBoard is running a pretty sophisticated and costly microcontroller. The Digi-Key pricing for the STM32F405RGT6 puts it in the \$7.57 range for volumes of 1k. Most of the processing power is undoubtedly "wasted" running Micro Python

and a MCU of half the cost could probably be used especially in medium to high volume applications.

What's interesting about Micro Python is that it follows the [MIT software license](#) and is freely available on [github](#) for ports and modification. Selecting a slightly less capable MCU such as the STM32F401RE would halve the cost (along with clock speed and a few other features) while still maintaining the integrity of the Micro Python system. The software development costs in C for a cheaper MCU might not be up to the challenge of matching Micro Python.

Sceptical? I was too until I installed Micro Python to a STM32F4401RE Nucleo board running at 84 MHz. Using proper design techniques, I still found that Micro Python was performing in real-time and meeting all of the deadlines I was throwing at it. Perhaps the kitchen sink still hasn't been thrown at it, but it has survived a basic shake-down thus far. The process of installing Micro Python on the Nucleo Board took no more than a few hours thanks to stepping stones and great documentation left by a contributor.

Can Micro Python compete with or usurp C? There is certainly a strong case for moving up the ladder to a higher level, object oriented programming language. Overall development costs

are still a grey area, though, especially for high volume projects.

Micro Python will undoubtedly find a home amongst hobbyists and professionals looking to rapid prototype an embedded system. Micro Python may even find a home amongst low to medium volume production systems. But one thing is for certain: embedded software developers are in dire need of new tools to help them navigate the quagmire of embedded system design in the 21st century. Micro Python might just be one of the tools developers have been looking for.

Going Further

Check out the Micro Python website and documentation [here](#).

Jacob is putting together a series of videos on Micro Python that can be seen on his YouTube channel [here](#).

Jacob Beningo is a Certified Software Development Professional (CSDP) whose expertise is in embedded software. He works with companies to decrease costs and time to market while maintaining a quality and robust product. Feel free to contact him at jacob@beningo.com, at his website www.beningo.com, and sign-up for his monthly Embedded Bytes Newsletter [here](#).

ENERGY HARVESTING

ENERGY IS EVERYWHERE – AND NOW IT CAN BE HARVESTED EASILY

By Franck Perronnet, Analog Devices

Adopting an ambient energy harvesting solution in order to power sensors may generate sizeable savings. This sort of operation has recently become simpler, with the advent of dedicated ICs which can charge a storage unit using the energy available from by photovoltaic cells or thermoelectric generators.

Networks of sensors, which are commonly used with connected objects, are able to operate without batteries or electricity, through the implementation of energy harvesting. The result is a sizeable decrease, not just in the cost of the batteries themselves, but also in the cost of replacing them, a cost that can escalate with hard-to-access batteries. A good example is the batteries which power a gas flow measurement sensor installed in a pipeline.

There are some instances where a battery is not necessary, for example there are systems which have a power source able to exploit differences in temperature, light, vibrations, or any other mechanical principle that can provide energy. Examples include linear or optical smoke detectors which are spread across a forest to detect a fire as quickly as possible after it breaks out. These systems may be powered

by energy harvested from natural light, which is stored in a charging unit.

Vibration sensors can be distributed along

road and rail bridges providing feedback to determine whether repairs are needed to prevent road safety risks. For both examples a very large number of sensors are used which all use



Diagnostic platform based on the ADP5090, with an Ambeon solar panel and CO₂ (Cozir), humidity, and temperature sensors. Not only can it be used for its energy harvesting capabilities, but also as a full system for a diagnostic.

ENERGY HARVESTING

radio communication. In such cases, periodically replacing the batteries is too complicated and expensive.

Constantly increasing energy efficiency

Today, industry has reached a point where natural energy harvesting solutions are not only possible, but economically viable and often beneficial. This is down to a combination of increasingly efficient photovoltaic cells and thermoelectric generators, more available voltage regulators that provide a high efficiency from a low charge, and a wide range of micro-controllers and ISM-band RF circuits that have ultra-low consumption.

From the perspective of Analog Devices, the earliest markets for renewable energy harvesting are the Internet of Things, through networks of wireless sensors (temperature, humidity, presence) such as for smart buildings, portable devices intended to monitor vital signs, and portable devices designed for consumer markets such as wearable electronics. The photo (above) illustrates an example of a system diagnostics kit using environmental sensors (CO₂, humidity, temperature) powered by a light source. Its central unit is the ADP5090, an ultra-

low-power boost regulator with an algorithm to look for the point corresponding to the highest power provided (MPPT, Maximum Power Point Tracking) by the source.

Renewable energy sources include photovoltaic sources, such as sunlight and indoor light, and thermoelectric generators (Peltier effect) that operate on variations in temperature. Piezoelectric vibration energy sources are also possible, if a regulation solution is used that has a wider (i.e. greater) input voltage than the ADP5090.

With such a circuit, the energy harvested is converted by the boost regulator before being stored in a traditional capacitor, a supercapacitor, or a Li-ion battery. Circuitry to protect against an overload of the charging unit or a deep battery discharge is included.

The article continues (click link) by outlining the calculations of available energy in different circumstances, and follows the process of correctly sizing the photovoltaic cells to the application.



LED Lighting



**Download PDF
of Article**



**Find Energy Harvesting
on EETsearch**

DON'T GET CAUGHT OUT BY CHANGING ENERGY EFFICIENCY REGULATIONS

By Jeff Schnabel, CUI Inc.

While the harmonisation of energy efficiency standards is an obvious goal that benefits international trade, the existence of various regulatory bodies around the globe continues to make this a game of leapfrog.

Currently, in the sphere of external power supply efficiency, Europe leads the world with the most stringent legislation that implements the Level V Marking Protocol. However from February 10, 2016 the baton will pass to the USA whose Department of Energy will then require all domestically (i.e. domestic US) manufactured or imported external power supplies to meet the new Level VI Efficiency Standard.

Consequently it is imperative that any manufacturer of equipment that relies on external power supplies, and whose product might be destined for the US market, is aware of these regulatory changes in time to ensure compliance without disruption to its supply chain. This may seem obvious but it's not necessarily the reality of the situation, as we'll see from the case study below of a European manufacturer whose products end up with American customers through a variety of sales channels.

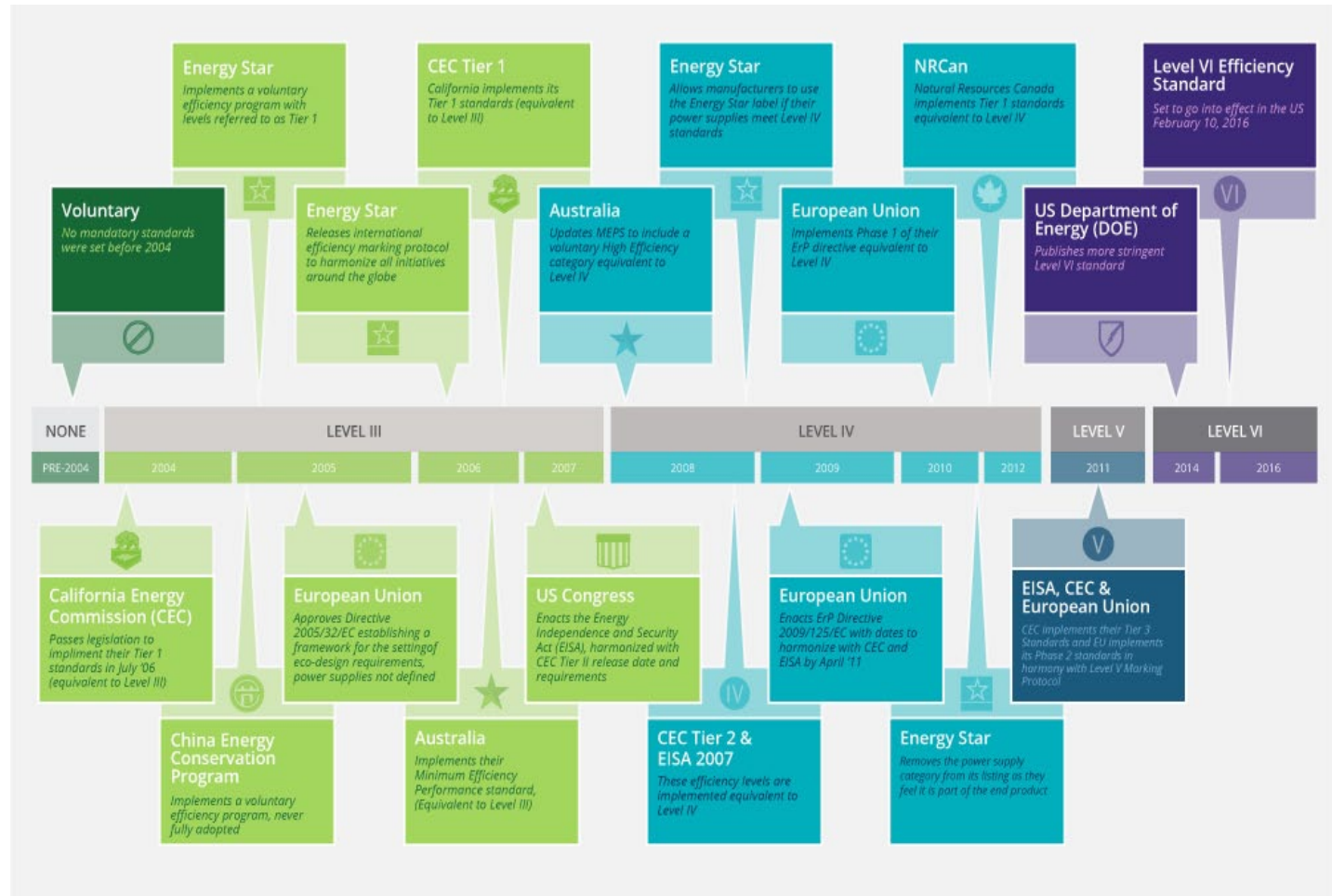


Figure 1. The regulatory timeline that has led to the present (impending) Level-VI regulations. (Source; CUI Inc. website)

POWER SUPPLIES

What's different in Level VI?

This is the immediate question a European manufacturer, who will already be aware of EU Phase 2 efficiency standards for external power supplies and the Level VI Marking Protocol, needs to understand. Superficially it might seem that an equipment maker who simply bundles an external power supply with its end-product only needs to procure a Level VI compliant power adapter to ship to its US customers after February 10, 2016.

Of course, life is never that simple! The scope of the new regulations is broader and the specifications are more complex than the previous Level IV and Level V requirements. For example, multi-output power supplies and supplies rated at over 250W are now included, meaning the legislation will embrace more applications than before and extend into areas not typically thought of as portable equipment, such as lighting installations that use external power supplies.

Other, less obvious, implications arise from the tighter efficiency limits and the way that Level VI now segments the different classes of external supply, with separate specifications for



AC/DC and AC/AC, and distinguishes between low-voltage types that output less than 6V and basic-voltage types with outputs greater than 6V. For the system vendor this may force a different choice of adapter to kit with its equipment, which if nothing else may have different mechanical dimensions to the previous unit even if the essential electrical parameters (voltage and current ratings) remain unchanged. In many instances simply re-engineering power supply designs to meet the tighter efficiency specifications is likely to result in a larger form factor.

Click for the continuation of this short article, that includes a case study of a manufacturer that needed an accelerated programme to update its PSUs.

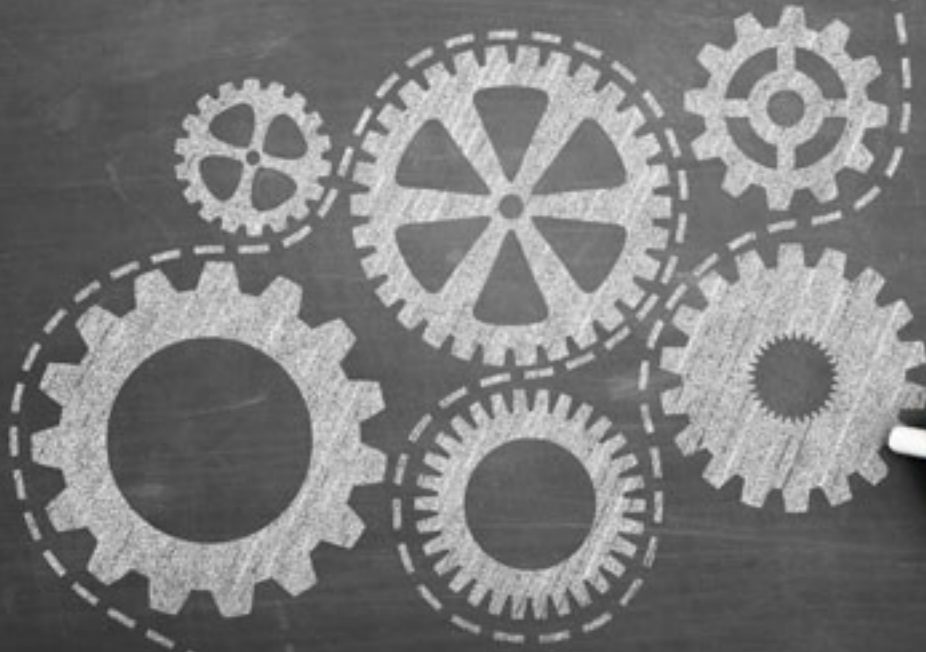


**Download PDF
of Article**




**Find Energy Efficiency
Regulations on EETsearch**

designideas



- Software PLL syncs to line using moving-average filter
- Isolated USB-to-UART converter builds in 20 minutes for \$20

Software PLL syncs to line using moving-average filter By Dobromir Dobrev

 A SPLL (software phase-locked loop) is used in this Design Idea to generate a synchronous reference to common-mode powerline interference in two-electrode ECG amplification. Though intended for ECG signal processing, it can easily be adapted to various DSP applications where frequency synchronisation is a must.

The basic SPLL structure consists of three blocks: Phase detector (PHD), Loop filter (LF), and Digitally-controlled oscillator (DCO) (Figure 1). The input signal V_{in} is processed in digital form: the PHD is a multiplier – its output, the product of two signals: the input sine wave (f_{in}), and the DCO sine output (f_{ref}). Sine wave mixing is preferable when low jitter is a must.

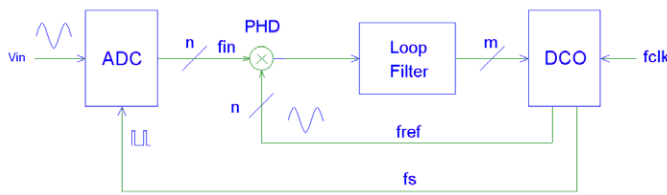


Figure 1. Software PLL structure

The LF integrates the PHD output data in time and increases the resolution due to averaging, so the m-bit wide DCO input can be larger than the n-bit wide signals.

The DCO operates as a digital-to-frequency converter with sine output, and must be able to match the expected input frequency range.

The key part of the SPLL is the loop filter. It must be carefully designed to provide stable system response with appropriate settling time.

Loop gain analysis and design methodology of the SPLL is given in Ref 1, where it is shown how the SPLL z-domain transfer function can be derived from its analogue s-domain prototype using backward difference s-plane to z-plane mapping.

The SPLL control loop consists of two integrators: one is hidden in the DCO, and another one is in the LF. Because the LF integrator serves a second integrator in the loop, it must be bypassed with a forward path to maintain stability, as seen in Figure 2. The disadvantage of this topology is that the forward path increases the remaining ripple at the DCO input, which is converted to jitter at the DCO output.

The problem can be overcome with a comb filter with notches at all powerline harmonics. The simplest comb filter rejecting all harmonics is a one-period moving-average filter (averager) [Ref 2]. Adding this to the loop greatly reduces the remaining ripple at the DCO input, and this is the heart of the Design Idea.

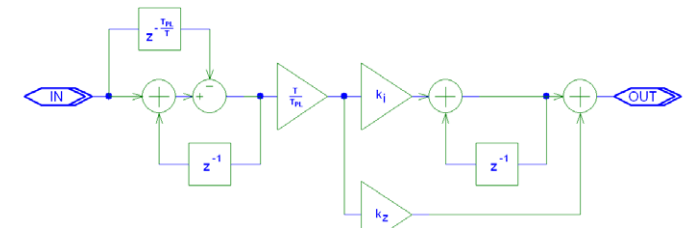


Figure 2. Loop filter structure

The LF transfer function is given with Eq. (1), where the first multiplicand is the transfer function of the averager, and the second multiplicand is the transfer function of the bypassed integrator:

$$LF(z) = \frac{T(1 - z^{-\frac{T_{PL}}{T}})}{T_{PL}(1 - z^{-1})} \cdot \frac{k_i + k_z(1 - z^{-1})}{1 - z^{-1}} \quad (1)$$

T is the sampling period: $T = 1/f_s$.
 TPL is the powerline period: $T_{PL} = 1/f_{PL}$.
 k_i and k_z are the gain coefficients in the integrator and in the forward paths.
 For sampling rate $f_s = 2$ kHz or $T = 0.5$ msec,
 $f_{PL} = 50$ Hz ($T_{PL} = 20$ msec), $k_i = 1/128 \approx 0.0078$,
 and $k_z = 8$
 Eq. (1) can be rewritten as Eq. (2):

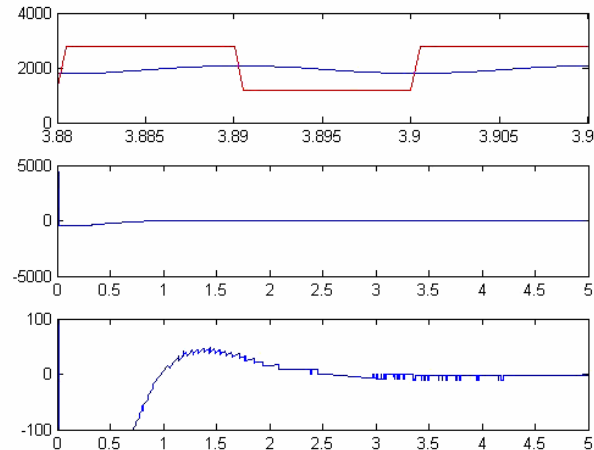
$$LF(z) = 0.025 \frac{1-z^{-40}}{1-z^{-1}} \cdot \frac{0.0078 + 8(1-z^{-1})}{1-z^{-1}} \quad (2)$$

The LF transfer function, given with Eq. (1), can be realised with the signal flow schematic shown in Figure 2.

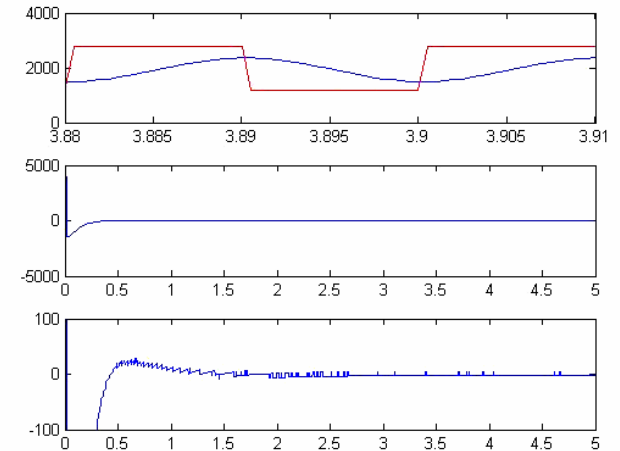
The SPLL is implemented and tested on the STM32F407 microcontroller, running at $f_{clk} = 100$ MHz. The microcontroller incorporates a 12-bit ADC which is used to convert the input signal at sampling rate $f_s = 2$ kHz. One LSB corresponds to $3V/4096 = 0.732$ V. The DCO range is ± 2 Hz. It is controlled with a 12-bit word; thus, the DCO sensitivity is 1 mHz/LSB, or 1.36 Hz/V. To avoid floating point multiplications, the DCO generates a 256-level sine wave. The mixer output is divided by 256 to set the correct loop gain. To minimise the DCO's remaining ripple, the ADC sampling rate is a multiple of the generated frequency f_{ref} . Thus, the averager, included in the LF, is maximally effective

in rejection the powerline harmonics.

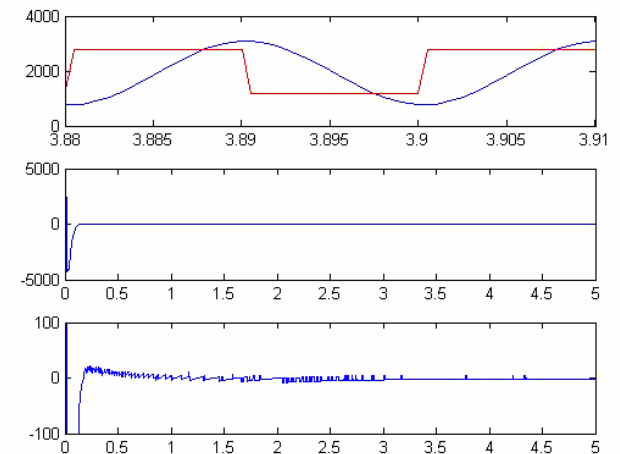
Figure 3 shows actual operation of the microcontroller. The data are transferred to a PC and visualised with MATLAB. The loop speed depends on the input signal amplitude. It can be seen that the DCO has a stable response with input amplitudes from 0.2 VP-P to 1.6 VP-P. Once the DCO input has settled, the generated rectangular waveform leads the input sine wave by 90 degrees.



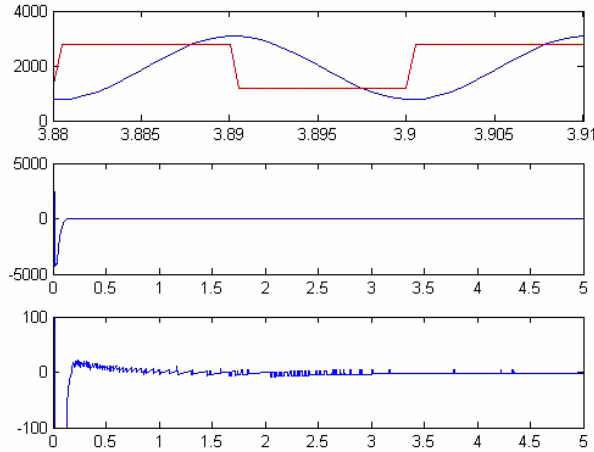
a) $V_{in}=0.2V_{pp}$, $f_{in}=50Hz$



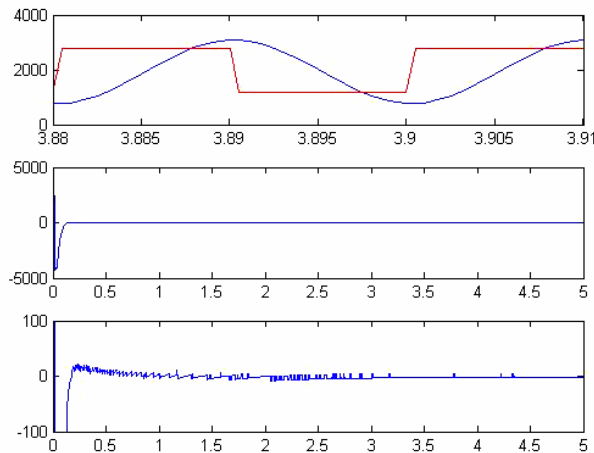
b) $V_{in}=0.6V_{pp}$, $f_{in}=50Hz$



c) $V_{in}=1.6V_{pp}$, $f_{in}=50Hz$



d) $V_{in}=0.6V_{pp}$, $f_{in}=49Hz$



e) $V_{in}=0.6V_{pp}$, $f_{in}=51Hz$

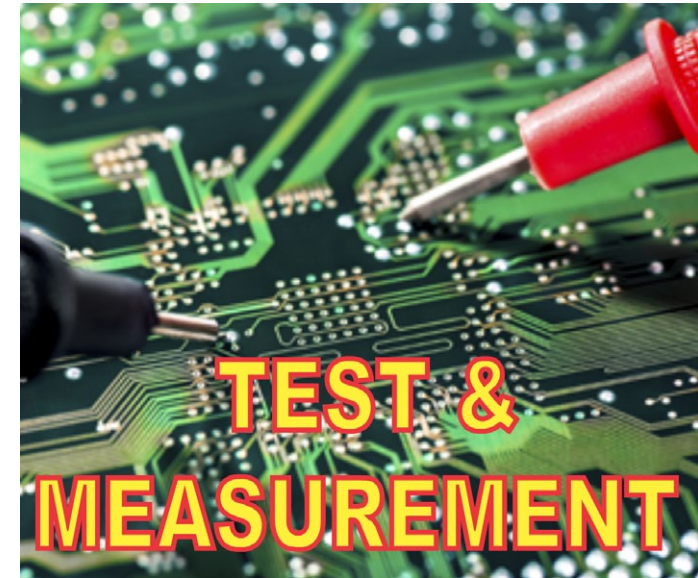
Figure 3. Practical results. For each image, the top display shows input & output signals. The second and third displays are the DCO input at different zooms.

– Download the [source code](#)

References:

Dobrev D., [Software PLL for power-line interference synchronization: Design, modeling and simulation](#), Annual Journal of Electronics, 2014
 Dobrev D., [Simulate digital filters with PSpice](#), EDN, 2015

Dr. Dobromir Dobrev has about 20 years experience in CMOS and BJT analogue and mixed-signal IC design (opamps, comparators, bandgaps, LDOs, filters, oscillators, LVDSs, PLLs, ADCs, etc.), as well as in signal processing in medical electronics (bioinstrumentation, bioamplifiers, biosignal filtering); in his career he has worked as an analogue IC designer at Semcotec Engineering, Silway Semiconductors, Megaxess and as a senior IC designer at Melexis. Currently, he is with FACET (Fabless Center for Engineering and Test), and lives in Sofia, Bulgaria. You can e-mail him at dpdobrev@gmail.com.



Isolated USB-to-UART converter builds in 20 minutes for \$20

By Jacob Beningo



I stood in stunned silence at the smoke billowing up from the hardware on the workbench. Just moments before, it had been operating as expected, before self-destructing with a sound that can only be compared with a gunshot. The failure of the hardware under test had an unexpected consequence: the computer that had been using a USB-to-UART converter to communicate with the hardware experienced a USB fault that was not recoverable. The computer was now damaged and worthless.

A simple isolation circuit that costs only a few dollars could have been used to protect the USB port on the computer. Embedded system developers get used to plugging strange hardware and components into their computers on a daily basis and rarely consider the consequences of what their actions might bring.

This Design Idea documents a low-cost, isolated USB-to-UART converter using the Sparkfun USB-to-UART breakout board (BOB).

There are a number of times when an isolated USB-to-UART converter can come in handy.

For example, during development of battery powered devices, there is a tendency to leave the USB-to-UART converter attached to the device, which, without isolation, will connect it through the host's ground to an Earth ground. The device may work perfectly, but when detached from the computer, it doesn't work at all. The isolated converter will keep the device and host grounds separate, allowing any grounding issues to be found early on rather than later.

The most important use of an isolated USB-to-UART converter is of course in fault conditions. Consider the consequences of connecting an untested electronic board to an expensive laptop such as a MacBook Pro. The USB specification and hardware layer does have protection circuits, but they may not be rated for devices operating at hundreds of Volts DC. When a device fails on the USB bus and has the potential to put more than 5V, or significant current, onto the bus, it is a wise decision to spend \$20 and isolate the two devices.

Selection of an isolator

The isolator selection requires careful consideration. UARTs have traditionally been con-

sidered low speed devices but modern micro-controllers and interfaces can support baud rates in excess of 1 Mbps. Many isolators, especially opto-isolators, have maximum baud rates under 100 kbps. The SI8421BB-D-IS from Silicon Labs turns out to be a really good match to this application, but is no longer recommended for new design. An alternate is the ADUM3211ARZ, but this part was not tested, so use at your own risk.

The SI8421BB supports 2.5 kV of isolation for 1 minute. The BB designation shows that the isolator is capable of baud rates up to 150 Mbps. The low volume cost for the SI8421BB-D-IS is only \$1.46, but if that is too expensive then the SI8421AB-D-IS is only \$1.05 (with a maximum baud rate of 1 Mbps). Another advantage of the SI8421BB-D-IS is that it has two isolators in the 8-pin SOIC package, which is perfect for a Tx/Rx signal pair. The isolators are unidirectional, but laid out such that they are pin-compatible with the Sparkfun USB-to-UART BOB if proper care is taken.

Building one

There are a small number of parts that need to be ordered:

| Quantity | Component | Source | Part Number | Price |
|----------|------------------------|----------|----------------------|---------|
| 1 | USB-to-UART | Sparkfun | BOB-12731 | \$14.95 |
| 1 | SOIC Breakout | Sparkfun | BOB-00494 | \$2.95 |
| 1 | 0.100 in.Headers | Sparkfun | PRT-00116 | \$1.50 |
| 1 | SI8421BB-D-IS Isolator | Digikey | 336-1756-5-ND | \$1.46 |

The total cost for these components is around \$20 plus shipping. Most developers have at least one project running at a time so purchasing enough material to build two or three units helps to offset the shipping cost. The complete set of components should look similar to that of Figure 1.

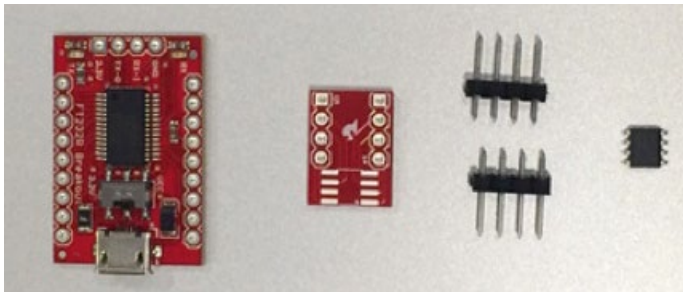


Figure 1. Isolated USB-to-UART components

Assemble the isolator

Start by soldering the isolator to the SOIC BOB (Figure 2). Then, add headers to both boards as shown in Figure 3.

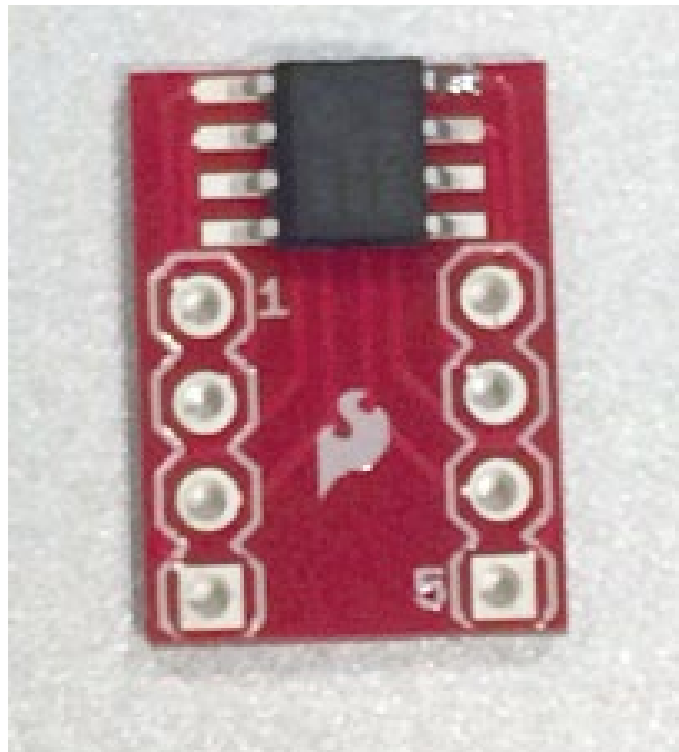


Figure 2. SOIC-8 BOB preparation

The USB-to-UART BOB requires a four pin header where Gnd, Tx, Rx, & VCC are located.

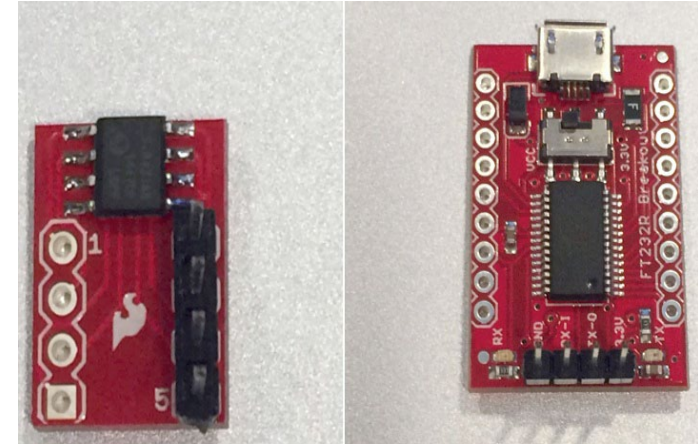


Figure 3. Header placement

The isolation board can now be soldered directly to the USB-to-UART BOB. Pin 1 of the SI8421BB-D-IS is power and should be aligned with the 3.3V that is supplied by the FTDI232R IC on the converter board. The assembly of the isolated USB-to-UART converter is now complete!

....continues next page

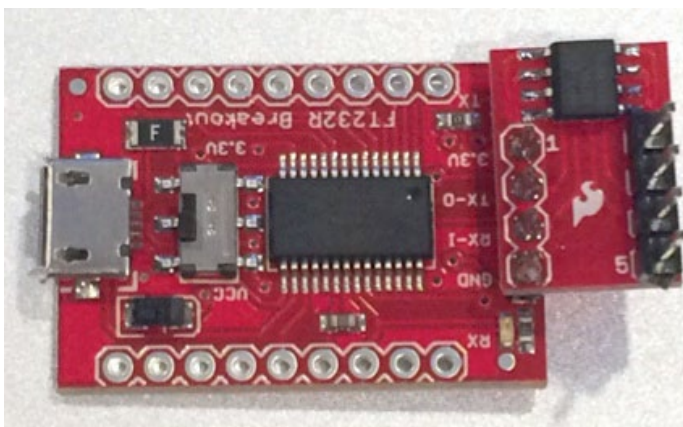


Figure 4. Assembled isolated USB-to-UART converter

Testing the converter

The USB-to-UART board is powered by USB 5V through the USB cable that is connected to the host. The onboard FTDI232R outputs 3.3V which powers side 1 of the isolator. Side 2 needs to be powered by the DUT's hardware, and can be either 3.3 or 5 volts. The easiest way to test the isolated converter is to supply power and ground to side 2 of the SI8421BB-D-IS and then create a loopback by connecting Tx to Rx. The nice thing about the isolation board setup is that the unlabelled pins on the SOIC-8 BOB directly correlate to the USB-to-UART silkscreen, so that Vcc, Tx, Rx, and GND are all aligned.

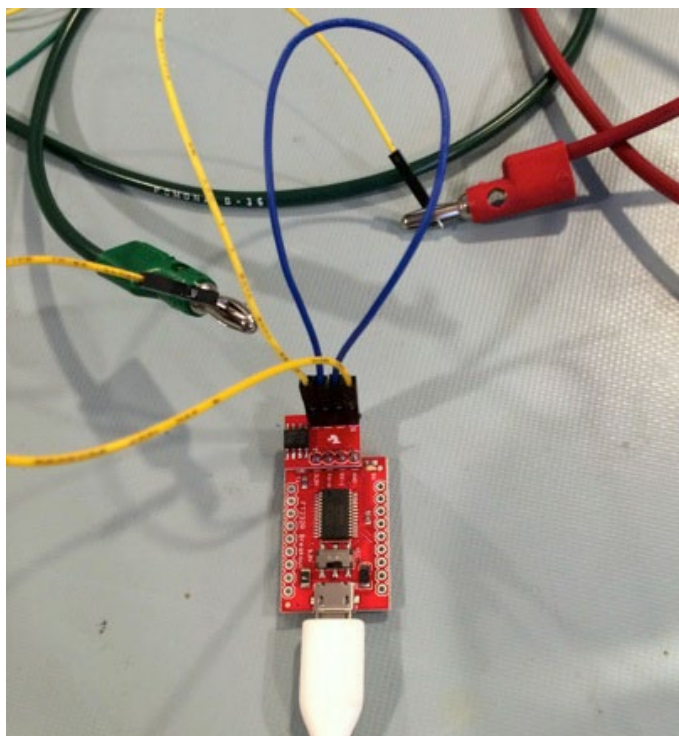


Figure 5. Testing the converter

Finally it is time to test the board. Fire up your favourite terminal application and open the VCP (virtual COM port, as created by the FTDI device driver). Just to push the limits, I set my terminal to the maximum of 921.6 kbps. Typing into the terminal should send data out the isolator, which loops it back in, and characters should appear on the terminal (Figure 6). If problems arise, the USB-to-UART board does have Tx and Rx LEDs onboard. Typing in the terminal should illuminate both. If one of them

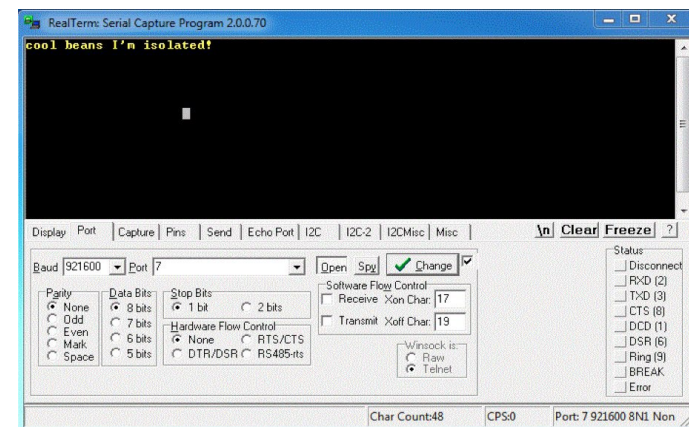


Figure 6. Loopback test of the isolated USB-to-UART converter

is not lighting up, then you know which side of the isolator to start looking for problems on.

Final thoughts

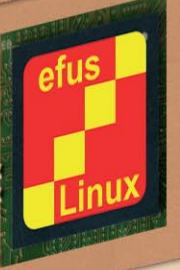
At a minimum, building this simple isolation board helps to provide protection that wasn't there in the first place. As a further ruggedising step, you could add ESD protection to the UART side.

A video that goes through the assembly process in even greater detail can be found [here](#).

Jacob Beningo is a Certified Software Development Professional (CSDP) who specialises in the development and design of quality, robust embedded systems. As a consultant, Jacob has worked in various industries including Automotive, Consumer, Defence, Medical and Space.



productroundup



BLDC motor control MCU has built-in pre-driver

This IC is presented as the smallest vector control microcontroller that incorporates Toshiba's Vector Engine Plus (VE+) coprocessor and a pre-driver to enable brushless DC motor control. The TMPM37AFSQG pre-driver can directly drive MOSFETs for complementary three-phase



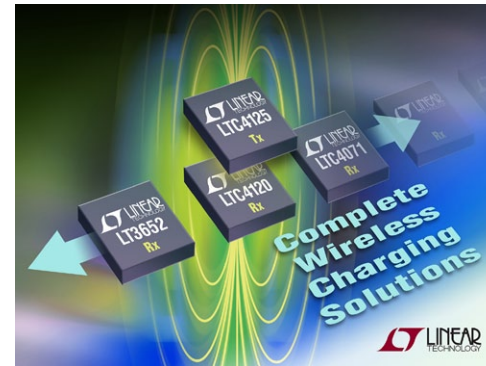
PWM output with a minimum unit of 25 nsec; it has an ARM Cortex-M3 core at up to 40 MHz, a 12-bit A/D converter and an on-board vector control platform. Also integrated into the device are an op-amp for current detection using a single shunt resistor and a comparator for over-current detection.

[Complete article, here](#)



5W AutoResonant wireless power Tx with FOD

LTC4125 is a wireless power transmitter configured as a simple, high performance monolithic full bridge resonant driver, capable of delivering up to 5W of power wirelessly to a companion receiver. The LTC4125



automatically adjusts its drive frequency to match the LC network resonant frequency. This AutoResonant switching enables the device to deliver maximum power from a low voltage input supply (3V to 5.5V) to a tuned receiver such as Linear's LTC4120 wireless receiver and battery charger via loosely coupled coils.

[Complete article, here](#)



Constant impedance from SPDT RF switch

IDT's F2923 provides constant impedance on all ports during switching transitions without compromising isolation, linearity or insertion loss. Positioned as the first single-pole, double-throw (SPDT) RF switch



featuring IDT'S KZ constant impedance technology, The IDT F2923 is a low insertion loss SPDT absorptive RF switch; from 300 kHz to 8000 MHz, IDT's KZ technology ensures the device delivers near-constant impedance (VSWR < 1.4:1 compared to 9:1 for standard switches) when switching from one RF port to another.

[Complete article, here](#)



Low power PIC MCUs eliminate external memory

Microchip's PIC24F "GB6" microcontroller family has dual-partition flash with live update, for always-on capability; it is the first 16-bit PIC MCU with up to 1 MB of flash with error correction code (ECC) and 32 kB RAM, which can eliminate external memory and support low-power



operation. Featuring dual-partition flash with live update capability, active current consumption is as low as 190 μ A/MHz and 3.2 μ A in Sleep mode. Over-the-air firmware updates provides a cost-effective, reliable and secure method for updating applications.

[Complete article, here](#)



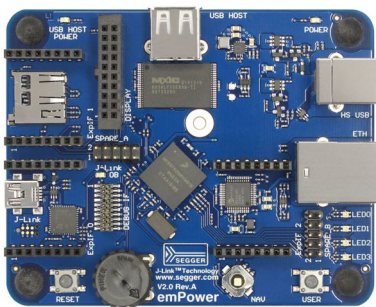


productroundup

ARM-based demo board for software evaluation

The emPower evaluation board from Segger (Hilden, Germany) is a vehicle to explore the company's embedded software offerings and accelerate the start of an embedded project. emPower is, Segger says, an affordable platform for customers to enhance software evaluation, prototyping and proof of concept.

Segger's embOS real-time operating system is at the heart of the evaluation; trial versions of the emFile file system, emWin graphics library, emUSB Host & Device, and embOS/IP TCP/IP stack (including web server demo) enable full use of the emPower peripherals.



Complete article, here



Sub-1-GHz, wireless MCU has 20 km range

Texas Instruments' SimpleLink Sub-1 GHz CC1310 wireless MCU, ultra-low power platform is designed to add ultra-low power, long-range connectivity to Internet of Things (IoT) designs. The sub-1 GHz CC1310 wireless microcontrollers (MCUs) offers up to 20 years of battery life for building and factory automation, alarm and security, smart grid and wireless sensor network applications. The MCUs feature: extended battery life with an ultra-low power radio, integrated ARM Cortex-M3 MCU core, sensor controller, low-power modes and 0.6 μ A sleep current, with ULPBench [EEMBC] score of 158.



Complete article, here



Code analysis with functional safety tools for ARM

IAR Systems is extending the features and device support in the functional safety edition of IAR Embedded Workbench for ARM, certified according to IEC 61508, EN 50128, and ISO 26262. The latest version of the functional safety edition embedded development toolchain has a build chain certified by TÜV SÜD as a qualified tool for development of safety-related applications. The new version integrates IAR Systems' C-STAT and C-RUN add-on tools for static and runtime code analysis. IAR Embedded Workbench for ARM has been tested and approved according to the requirements on support tools embodied in IEC 61508, as well as ISO 26262, which is used for automotive safety-related systems and EN 50128, the European railway standard. C-STAT features static analysis that can detect defects, bugs, and security vulnerabilities as defined by CERT and the Common Weakness Enumeration, as well as help keeping code compliant to standards such as MISRA C:2012/2004 and MISRA C++:2008.

Complete article, here



5000 μ F capacitor, embedded in a smartcard

An electric double-layer capacitor from TDK presents 5000 μ F capacitance in a package with a maximum thickness of 0.45 mm, enabling it to be used as the power source for small e-paper displays and advanced biometric authentication systems. EDLC041720-050-2F-13 is an ultra-thin, high-energy capacitor electric double-layer capacitor with a footprint of 27 x 17 mm that can be mounted inside a smart card or other thin device. When fully charged, it provides around 50 mJ of energy to power a load. In smart cards, it is compatible with radio-frequency energy harvesting circuits.



Complete article, here





productroundup

IoT WiFi connectivity via social platform

Atmel has disclosed a path to ultra-low power Wi-Fi connectivity to the WeChat IoT platform, enabling secure cloud access for IoT applications. Using the Atmel | SMART SAM W25 SmartConnect module, the WeChat IoT platform supports the latest Airkiss 2.0 protocol for Wi-Fi provisioning and service discovery, allowing developers of connected devices to seamlessly connect to the cloud. Atmel is collaborating with WeChat, the social communication platform, on its IoT Platform with the SAM W25 module integrating a secure ATECC508 CryptoAuthentication, for cloud access targeting IoT applications. WeChat IoT Platform delivers cloud services for seamless accessibility to the Internet (“cloud”) ensuring every ‘thing’ is smartly connected. The platform, which is currently available in China, delivers a complete edge node-to-cloud solution from a single vendor for IoT developers.

Complete article, here



Class-H amp: richer sound from smaller devices

A smart amplifier enables, TI says, deeper, richer and louder audio for next-generation smartphones. The low-power smart amplifier aims to allow designers to develop next-generation smartphones with leading audio quality at peak volumes while maximising battery efficiency. The

New smart amplifier enables big sound from small devices

- Fully integrated speaker protection
- Ultra-low noise without compromise
- Intuitive tools to accelerate design



TEXAS INSTRUMENTS

TAS2555 Class-H audio amplifier with integrated speaker protection uses back electromotive force delivering 5.7W output power into 4Ω and 3.8W into 8Ω at 4.2V; low idle-channel noise (ICN) simplifies designs: 15.9-μV ICN eliminates audible speaker noise when using the smartphone in a receiver or pause mode.

Complete article, here



Dual-band FPC antennas for Wi-Fi and ISM

Antenna, manufacturer of antennas and RF antenna modules for M2M and the Internet of Things, has added three flexible FPC antennas for applications in industrial and consumer electronics. Two of the antennas, named Dromus and Amoris are high performance dual band Wi-Fi antennas operating on the 2.4-2.5GHz and 4.9-5.9GHz wireless bands, including Wi-Fi 802.11a/b/g/j/n/ac.

They are suitable for access points, portable electronics, PC cards, games consoles, set-top boxes, network devices, and wearable technology. The third antenna, named Montana, operates in the ISM bands of 863-870 MHz and 902-928 MHz.



Complete article, here



ARM extends mbed to aid IoT deployment

ARM is releasing a suite of products to accelerate secure IoT technology deployments on a large scale by businesses; ARM mbed IoT Device Platform. The release also includes the enhanced mbed OS (Technology Preview version) and new mbed Reference Designs. The products will shorten hardware design time, giving innovators greater ability to focus on product differentiation. mbed Device Connector allows developers to connect devices within prototype deployments, build secure web applications quickly and integrate them with cloud solutions. mbed Device Connector is free for developers to use on up to 100 devices, handling up to 10,000 events per hour. mbed OS Technology Preview version is the latest iteration of the modular, efficient OS for Cortex-M based MCUs. Built to enable the IoT to scale, developers can take advantage of product innovations including mbed TLS, a native OS support for Thread and basic manageability of devices.

Complete article, here





productroundup

Servo SoC accepts digital & analogue sensors

Under its C2000 Delfino branding, Texas Instruments has combined microcontroller and DesignDRIVE Position Manager technology to eliminate challenges in interfacing with position sensors in industrial servo and AC inverter drives. Positioned as the first on-chip solution supporting both analogue and digital position sensors, TMS320F28379D and TMS320F28379S microcontrollers (MCUs) enable simple interfacing to position sensors. System performance is improved by completing the decode tasks on-chip and reducing the communication latency, enabling faster control loop performance.



Complete article, here

Ref. design: 24-bit signal chain for industrial sensors

Industrial automation engineers can achieve highly accurate measurements for their system designs with the MAXREFDES67# analogue front end (AFE) universal input Micro PLC reference design from Maxim. As high-resolution systems move to higher bit counts, they become more sensitive to noise. The 24-bit AFE reference design overcomes this challenge. Capable of accepting four different signals, the universal analogue input requires no jumpers and is 100% software configurable. The design yields high accuracy: effective resolution up to 22.3 bits with temperature error as low as $\pm 0.1\%$ across a range of -40 to $+150\text{C}$.

24-Bit Universal Input Micro PLC MAXREFDES67



Complete article, here

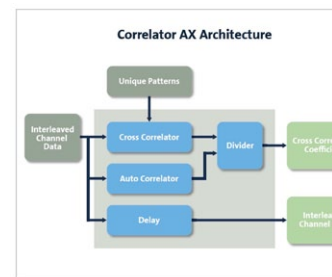
Free cloud-connected OS to boost IoT progress

Wind River is growing its presence in the cloud, and extending the scope of its OS at the “edge”, beyond devices and gateways, to microcontrollers (MCUs). Wind River Helix Cloud is a family of software-as-a-service (SaaS) products providing anytime, anywhere access to development tools, virtual labs, and deployed devices. Wind River Helix App Cloud is a cloud-based development environment for building IoT applications; Wind River Helix Lab Cloud is a cloud-based virtual hardware lab for simulating and testing IoT devices and complex systems; Wind River Helix Device Cloud is a cloud-based platform for managing deployed IoT devices and their data. A critical component of simplifying edge-to-cloud development is having an OS that can support connectivity and communications between the device and the cloud. Based on Wind River commercially proven OS technology and expertise, free cloud-connected operating systems are also available.

Complete article, here

Correlator IP for FPGA scans many data streams

RFEL (Newport, Isle of Wight, UK) has announced a multi-channel, multi-rate correlator deliverable as IP. The Correlator AX core offers high sensitivity Unique Pattern (UP) detection from multiple, interleaved data streams with differing sample rates; it provides the ability to simultaneously analyse thousands of input channels obtained from different carriers in real time using advanced parallel processing. It can search for up to two Unique Patterns (UPs) on each channel and provides reliable identification with a low False Alarm Rate using both cross-correlation and auto-correlation.



Complete article, here

BRIAN'S BRAIN

ANTICIPATING CES 2016: WEARABLE DEVICE DISPLAY TRENDS

BY BRIAN DIPERT

Wearable devices were, as I predicted in advance, one of the big hits of the early-March MWC (Mobile World Congress) show. This fact might be a surprise to some, who recall it as historically being a cellphone-centric conference. However, most of today's wearables are, at minimum, tetherable companions to smartphones. And an increasing number of them are cellular data-cognizant in their own right. If wearables' presence at MWC was a surprise, their further proliferation at the upcoming CES (Consumer Electronics Show) shouldn't be. Although new players may enter the space in January, and new products certainly will appear, the product categories themselves are fairly fixed at this point: activity trackers and smart watches, supplemented by lower-volume body cameras, smart glasses and other augmented reality headsets, and the like. The appearance of revolutionary new wearable product categories is therefore of less interest to me than is evolution within each category. And one of the evolutions-or-not that I'll be watching most closely involves display technology. There's a lot to like about my [Moto 360 smart watch](#), for example, particularly now that I've paired it with an Android handset. When properly backlit, for example, its LCD is ab-

solutely gorgeous, and since I exclusively use the black-background "minimal" watch face, I don't even notice the "flat tyre" area that houses the ambient light sensor and other electronics. About that LED backlight and ambient light sensor, however ... together, they represent my biggest "beef" with the product. For understandable battery life reasons, Motorola is motivated to keep the backlight as dim as possible, ideally off, as often as possible. The backlight is supposedly activated by the owners' wrist motion, suggestive of a glance at the watch face; in my experience, this accelerometer-sensed function is hit-and-miss at best. And when the backlight is activated, its brightness is modulated by ambient light sensor determination; again, in my experience, this



capability regularly undershoots intensity necessity (a requirement that's admittedly accentuated by my presbyopia). The Moto 360 offers an off-by-default "ambient screen" mode that dampens the usual backlight-disable aggressiveness, but you're warned when you attempt to switch it on that "Ambient screen reduces battery life." Caveat emptor, as they say. OLEDs are a perhaps obvious alternative to LCDs, but as I've repeatedly mentioned before in both technical articles and blog posts, they come with associated tradeoffs. The lack of a backlight can improve battery life; black pixel-dominant OLED display outputs are even more power-efficient. Wide viewing angles and (theoretically, at least) cost-effective manufacturing processes are among OLED's other upsides.

BRIAN'S BRAIN

However, that same backlight-less attribute also leads to display wash-out in bright ambient light settings, such as direct sunlight. And OLEDs don't last as long as do LCDs; while limited lifetime is perhaps not a concern in a low-cost device that'll be obsolete in a year or so, it's a bigger issue with a high-end smart watch, not to mention a television.

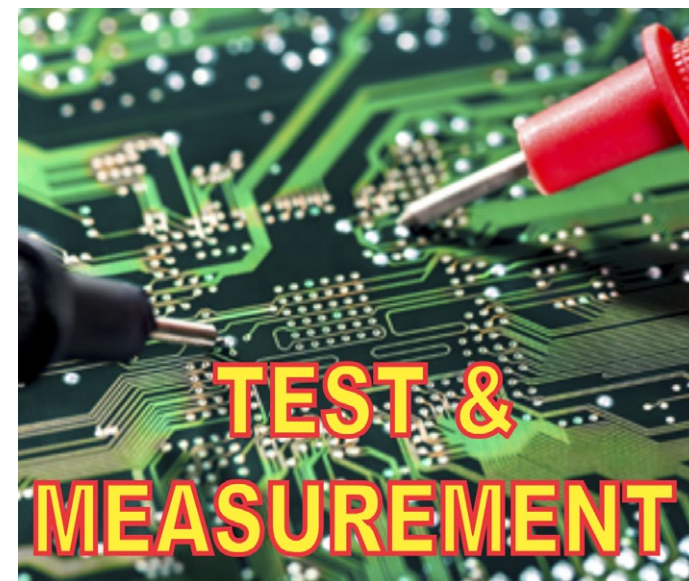
Then there's electrophoretic ink (**E ink**), the display technology most notably employed in the Amazon Kindle series and other e-book readers. Since they "hold static text and images indefinitely without electricity," to quote Wikipedia, electronic paper technologies like these are quite appealing for use in wearables from a battery life standpoint. But they're nominally only capable of displaying grey-scale pixels (via clusters of monochrome sub-pixels); some approaches (such as Qualcomm's Mirasol) are also capable of delivering full-colour (albeit limited-range) detail. Most notably, it finds use in Pebble's new Time, Time Steel and **Time Round** smart watches.

It's increasingly evident to me as I pore through product reviews and market forecasts that some sort of display (and not just a few embedded LED status lights, by the way) will increasingly be necessary in wearables, with the possible exception of very entry-level product variants. Most consumers, for example, dislike the need to download a display-less activity band's data to a smartphone or computer

in order to be able to peruse it. Conversely, consider the meaningful amount of information directly delivered by Microsoft's (admittedly more expensive) **Band** or counterparts from other suppliers. But which display technology will dominate long-term?

The likely answer is "it depends." But ironically, I don't believe it includes continued dominance of today's popular LCD. While I don't discount the cost advantages of a mature, widely adopted technology, and much as I love the richness of the display built into my Moto 360, the necessity for a backlight is a deal-breaker from a battery life standpoint. The structural rigidity of that same backlight also results in limitations in both system form factor and function versus with, say, an OLED-based alternative.

Between OLED and E ink, the fundamental decision will likely come down to image quality versus battery life. Personally, I find it mildly (or more) annoying to have to recharge my LCD-based smart watch every night. With an OLED-based alternative, I might be able to stretch it out to two days between charges ... still too often for my tastes. But then again, I've been wearing wristwatches all my life, and am therefore used to months or years of operation between battery replacements. Someone who's coming at a smart watch having never worn a watch before, but is already used to plugging in various widgets every night for recharging purposes, might not have the same objections.



EDN

europe

EDN-EUROPE is published 11 times in 2015 by
European Business Press SA,
533 Chaussée de Louvain, 1380 Lasne, Belgium
Tel: +32-2-740 00 50 Fax: +32-2-740 00 59
email: info@eetimes.be.
VAT Registration: BE 461.357.437.
RPM: Nivelles.
It is free to qualified engineers and managers
involved in engineering decisions – see:
<http://www.edn-europe.com/subscribe>
Copyright 2015 by European Business Press SA.
All rights reserved. P 304128

CONTACTS

PUBLISHER

André Rousselot
+32 27400053
andre.rousselot@eetimes.be

CIRCULATION & FINANCE

Luc Desimpel
luc.desimpel@eetimes.be

EDITOR-IN-CHIEF

Graham Prophet
+44 7733 457432
edn-editor@eetimes.be

ADVERTISING PRODUCTION & REPRINTS

Lydia Gijsegom
lydia.gijsegom@eetimes.be

Patrick Mannion

Brand Director EDN Worldwide

ART MANAGER

Jean-Paul Speliers

ACCOUNTING

Ricardo Pinto Ferreira



European
business press

SALES CONTACTS

Europe

Daniel Cardon
France, Spain, Portugal
+33 688 27 06 35
cardon.d@gmail.com

Nadia Liefsoens
Belgium
+32-11-224 397
n.liefsoens@fivemedia.be

Nick Walker
UK, Ireland, Israel,
The Netherlands
+44 (0) 1442 864191
nickwalker@btinternet.com

Victoria & Norbert Hufmann
Germany, Austria,
Eastern Europe
+49 911 93 97 64 42
sales@hufmann.info

Monika Ailinger
Switzerland
+41-41-850 4424
m.ailinger@marcomedia.ch

Andrea Rancati
Italy
+39-02-284 6716
info@silvera.it

Colm Barry & Jeff Draycott
Scandinavia
+46-40-41 41 78
jeff.draycott@womp-int.com
colm.barry@telia.com

USA & Canada

Todd A. Bria
West
+1 831 477 2075
tbria@globalmediasales.com

Jim Lees
PA, NJ & NY
+1-610-626 0540
jim@leesmedia.com

Steve Priessman
East, Midwest,
South Central
& Canada
+1-630-420 8744
steve@stevenpriessman.com

Lesley Harmoning
East, Midwest, South Central
& Canada
+1-218.686.6438
lesleyharmoning@gmail.com

Asia

Keita Sato
Japan
+81-3-6824-9386
Mlshida@mx.itmedia.co.jp

Grace Wu
Asian Sources Publications
Asia
(886-2) 2712-6877
wug@globalsources.com

John Ng
Asian Sources Publications
Asia
(86-755) 8828 – 2656
jng@globalsources.com